Technical Reference Guide

HP Compaq dc7900 Series Business Desktop Computers

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This document provides information on the design, architecture, function, and capabilities of the HP Compaq dc7900 Series Business Desktop Computers. This information may be used by engineers, technicians, administrators, or anyone needing detailed information on the products covered.

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1 Introduction

1.1 About this Guide

This guide provides technical information about HP Compaq dc7900 Business PC personal computers that feature Intel processors and the Intel Q45 Express chipset. This document describes in detail the system's design and operation for programmers, engineers, technicians, and system administrators, as well as end-users wanting detailed information.

The chapters of this guide primarily describe the hardware and firmware elements and primarily deal with the system board and the power supply assembly. The appendices contain general data such as error codes and information about standard peripheral devices such as keyboards, graphics cards, and communications adapters.

This guide can be used either as an online document or in hardcopy form.

1.1.1 Online Viewing

Online viewing allows for quick navigating and convenient searching through the document. A color monitor will also allow the user to view the color shading used to highlight differential data. A softcopy of the latest edition of this guide is available for downloading in .pdf file format at the following URL: www.hp.com

Viewing the file requires a copy of Adobe Acrobat Reader available at no charge from Adobe Systems, Inc. at the following URL: www.adobe.com

1.1.2 Hardcopy

A hardcopy of this guide may be obtained by printing from the .pdf file. The document is designed for printing in an 8 ½ x 11-inch format.

1.2 Additional Information Sources

For more information on components mentioned in this guide refer to the indicated manufacturers' documentation, which may be available at the following online sources:

- HP Corporation: www.hp.com
- Intel Corporation: www.intel.com
- Serial ATA International Organization (SATA-IO): www.serialATA.org.
- USB user group: www.usb.org

1.3 Serial Number

The serial number is located on a sticker placed on the exterior cabinet. The serial number is also written into firmware and may be read with HP Diagnostics or Insight Manager utilities.

1.4 Notational Conventions

The notational guidelines used in this guide are described in the following subsections.

1.4.1 Special Notices

The usage of warnings, cautions, and notes is described as follows:

WARNING: Text set off in this manner indicates that failure to follow directions could result in bodily harm or loss of life.

CAUTION: Text set off in this manner indicates that failure to follow directions could result in damage to equipment or loss of information.

Text set off in this manner provides information that may be helpful.

1.4.2 Values

Differences between bytes and bits are indicated as follows:

MB = megabytes

Mb = megabits

1.4.3 Ranges

Ranges or limits for a parameter are shown using the following methods:

Example A:	Bits <7..4> = bits 7, 6, 5, and 4.
Example B:	IRQ3-7, 9 = IRQ signals 3 through 7, and IRQ signal 9

1.5 Common Acronyms and Abbreviations

Table 1-1 lists the acronyms and abbreviations used in this guide.

Table 1-1
Acronyms and Abbreviations

Acronym or Abbreviation	Description
A	ampere
AC	alternating current
ACPI	Advanced Configuration and Power Interface
A/D	analog-to-digital
ADC	Analog-to-digital converter
ADD or ADD2	Advanced digital display (card)
AGP	Accelerated graphics port
AHCI	SATA Advanced Host controller Interface
AMT	Active Management Technology
API	application programming interface
APIC	Advanced Programmable Interrupt Controller
APM	advanced power management
AOL	Alert-On-LAN™
ASIC	application-specific integrated circuit
ASF	Alert Standard Format
AT	1. attention (modem commands) 2. 286-based PC architecture
ATA	AT attachment (IDE protocol)
ATAPI	ATA w/packet interface extensions
AVI	audio-video interleaved
AVGA	Advanced VGA
AWG	American Wire Gauge (specification)
BAT	Basic assurance test
BCD	binary-coded decimal
BIOS	basic input/output system
bis	second/new revision
BNC	Bayonet Neill-Concelman (connector type)
bps or b/s	bits per second
BSP	Bootstrap processor
BTO	Built to order
CAS	column address strobe
CD	compact disk
CD-ROM	compact disk read-only memory

Table 1-1 *(Continued)*
Acronyms and Abbreviations

Acronym or Abbreviation	Description
CDS	compact disk system
CGA	color graphics adapter
Ch	Channel, chapter
cm	centimeter
CMC	cache/memory controller
CMOS	complimentary metal-oxide semiconductor (configuration memory)
Cntlr	controller
Cntrl	control
codec	1. coder/decoder 2. compressor/decompressor
CPQ	Compaq
CPU	central processing unit
CRIMM	Continuity (blank) RIMM
CRT	cathode ray tube
CSM	1. Compaq system management 2. Compaq server management
DAC	digital-to-analog converter
DC	direct current
DCH	DOS compatibility hole
DDC	Display Data Channel
DDR	Double data rate (memory)
DIMM	dual inline memory module
DIN	Deutche IndustriNorm (connector type)
DIP	dual inline package
DMA	direct memory access
DMI	Desktop management interface
dpi	dots per inch
DRAM	dynamic random access memory
DRQ	data request
DVI	Digital video interface
dword	Double word (32 bits)
EDID	extended display identification data
EDO	extended data out (RAM type)
EEPROM	electrically erasable PROM
EGA	enhanced graphics adapter
EIA	Electronic Industry Association

Table 1-1 *(Continued)*
Acronyms and Abbreviations

Acronym or Abbreviation	Description
EISA	extended ISA
EPP	enhanced parallel port
EIDE	enhanced IDE
ESCD	Extended System Configuration Data (format)
EV	Environmental Variable (data)
ExCA	Exchangeable Card Architecture
FIFO	first in / first out
FL	flag (register)
FM	frequency modulation
FPM	fast page mode (RAM type)
FPU	Floating point unit (numeric or math coprocessor)
FPS	Frames per second
ft	Foot / feet
GB	gigabyte
GMCH	Graphics / memory controller hub
GND	ground
GPIO	general purpose I / O
GPOC	general purpose open-collector
GART	Graphics address re-mapping table
GUI	graphic user interface
h	hexadecimal
HDD	hard disk drive
HW	hardware
hex	hexadecimal
Hz	Hertz (cycles-per-second)
ICH	I / O controller hub
IDE	integrated drive element
IEEE	Institute of Electrical and Electronic Engineers
IF	interrupt flag
I / F	interface
IGC	integrated graphics controller
in	inch
INT	interrupt
I / O	input / output
IPL	initial program loader

Table 1-1 *(Continued)*
Acronyms and Abbreviations

Acronym or Abbreviation	Description
IrDA	Infrared Data Association
IRQ	interrupt request
ISA	industry standard architecture
Kb/KB	kilobits/kilobytes (x 1024 bits/x 1024 bytes)
Kb/s	kilobits per second
kg	kilogram
KHz	kilohertz
kV	kilovolt
lb	pound
LAN	local area network
LCD	liquid crystal display
LED	light-emitting diode
LPC	Low pin count
LSI	large scale integration
LSb/LSB	least significant bit/least significant byte
LUN	logical unit (SCSI)
m	Meter
MCH	Memory controller hub
MMX	multimedia extensions
MPEG	Motion Picture Experts Group
ms	millisecond
MSb/MSB	most significant bit/most significant byte
mux	multiplex
MVA	motion video acceleration
MVW	motion video window
n	variable parameter/value
NIC	network interface card/controller
NiMH	nickel-metal hydride
NMI	non-maskable interrupt
NRZI	Non-return-to-zero inverted
ns	nanosecond
NT	nested task flag
NTSC	National Television Standards Committee
NVRAM	non-volatile random access memory

Table 1-1 *(Continued)*
Acronyms and Abbreviations

Acronym or Abbreviation	Description
ODD	optical disk drive
OS	operating system
PAL	1. programmable array logic 2. phase alternating line
PATA	Parallel ATA
PC	Personal computer
PCA	Printed circuit assembly
PCI	peripheral component interconnect
PCI-E	PCI Express
PCM	pulse code modulation
PCMCIA	Personal Computer Memory Card International Association
PEG	PCI express graphics
PFC	Power factor correction
PIN	personal identification number
PIO	Programmed I/O
PN	Part number
POST	power-on self test
PROM	programmable read-only memory
PTR	pointer
RAID	Redundant array of inexpensive disks (drives)
RAM	random access memory
RAS	row address strobe
rcvr	receiver
RDRAM	(Direct) Rambus DRAM
RGB	red/green/blue (monitor input)
RH	Relative humidity
RMS	root mean square
ROM	read-only memory
RPM	revolutions per minute
RTC	real time clock
R/W	Read/Write
SATA	Serial ATA
SCSI	small computer system interface
SDR	Singles data rate (memory)
SDRAM	Synchronous Dynamic RAM

Table 1-1 *(Continued)*
Acronyms and Abbreviations

Acronym or Abbreviation	Description
SDVO	Serial digital video output
SEC	Single Edge-Connector
SECAM	sequential colour avec memoire (sequential color with memory)
SF	sign flag
SGRAM	Synchronous Graphics RAM
SIMD	Single instruction multiple data
SIMM	single in-line memory module
SMART	Self Monitor Analysis Report Technology
SMI	system management interrupt
SMM	system management mode
SMRAM	system management RAM
SPD	serial presence detect
SPDIF	Sony/Philips Digital Interface (IEC-958 specification)
SPN	Spare part number
SPP	standard parallel port
SRAM	static RAM
SSD	solid state disk (drive)
SSE	Streaming SIMD extensions
STN	super twist pneumatic
SVGA	super VGA
SW	software
TAD	telephone answering device
TAFI	Temperature-sensing And Fan control Integrated circuit
TCP	tape carrier package, transmission control protocol
TF	trap flag
TFT	thin-film transistor
TIA	Telecommunications Information Administration
TPE	twisted pair ethernet
TPI	track per inch
TTL	transistor-transistor logic
TV	television
TX	transmit
UART	universal asynchronous receiver/transmitter
UDMA	Ultra DMA

Table 1-1 *(Continued)*
Acronyms and Abbreviations

Acronym or Abbreviation	Description
URL	Uniform resource locator
us/µs	microsecond
USB	Universal Serial Bus
UTP	unshielded twisted pair
V	volt
VAC	Volts alternating current
VDC	Volts direct current
VESA	Video Electronic Standards Association
VGA	video graphics adapter
VLSI	very large scale integration
VRAM	Video RAM
W	watt
WOL	Wake-On-LAN
WRAM	Windows RAM
ZF	zero flag
ZIF	zero insertion force (socket)

2

System Overview

2.1 Introduction

The HP Compaq dc7900 Business PC personal computers (Figure 2-1) deliver an outstanding combination of manageability, serviceability, and compatibility for enterprise environments. Based on the Intel processor with the Intel Q45 Express chipset, these systems emphasize performance along with industry compatibility. These models feature a similar architecture incorporating both PCI 2.3 and PCIe 1.1 buses. All models are easily upgradeable and expandable to keep pace with the needs of the office enterprise.

Figure 2-1. HP Compaq dc7900 Business PCs

This chapter includes the following topics:

- Features (2.2)
- System architecture (2.3)
- Specifications (2.4)

2.2 Features

The following standard features are included on all models unless otherwise indicated:

- Intel processor in LGA775 (Socket T) package
- Integrated graphics controller with dual monitor support:
  - One VGA connector
  - One DisplayPort (DP) connector with Multimode support
- PC2-6400 and PC2-5300 (DDR2) DIMM support
- Hard drive fault prediction
- Eight USB 2.0-compliant ports
- High definition (HD) audio processor with one headphone output, at least one microphone input, one line output, and one line input
- Network interface controller providing 10/100/1000Base T support
- Plug 'n Play compatible (with ESCD support)
- Intelligent Manageability support
- Management/security features including:
  - Flash ROM Boot Block
  - Diskette drive disable, boot disable, write protect
  - Power-on password
  - Administrator password
  - Serial port disable (SFF and CMT form factors only)
  - Smart Cover (hood) Sense
  - Smart Cover (hood) Lock (SFF and CMT form factors only)
  - USB port disable
  - Intel Standard Manageability support
  - Intel vPro Technology
  - HP Virtual Safe Browser
- PS/2 enhanced keyboard
- PS/2 optical scroll mouse
- Energy Star compliancy met by all USDT form factors (Energy Star-qualified configurations of SFF and CMT form factors are available).

Table 2-1 shows the differences in features between the different PC series based on form factor:

Table 2-1
Feature Difference Matrix by Form Factor

	USDT	SFF	CMT
Processor types supported	Intel Celeron, Pentium dual-core, Core 2 Duo	Intel Celeron, Pentium dual-core, Core 2 Duo, Core 2 Quad	Intel Celeron, Pentium dual-core, Core 2 Duo, Core 2 Quad
Processor wattage (max)	65 W	95 W	95 W
Memory:			
# & type of sockets	2 SODIMM	4 DIMM	4 DIMM
Maximum memory	8 GB	16 GB	16 GB
Serial ports	0	1 std., 1 opt. [1]	1 std., 1 opt. [1]
Parallel ports	0	optional	optional
Drive bays:			
Externally accessible	1	2	4
Internal	1	1	2
Drive types supported	1 HDD, 1 slimline ODD	2 HDDs, 1ODD, RAID1	2 HDDs, 2 ODDs, RAID1
PCIe slots:			
x16 graphics (PCIe 2.0)	0	1 [3, 4]	1
x1 connector	1 [2]	1 [3]	1
x4 (x16 connector)		1 [3, 4]	1
PCI 2.3 32-bit 5-V slots	0	1 half-height or 2 full-height [5]	3 full-height
Power Supply Unit:			
Module type	external	internal	internal
power rating	135-watt	240-watt	365-watt

NOTES:

[1] 2nd serial port requires optional cable/bracket assembly.

[2] PCIe Mini Card slot.

[3] Supports low-profile card in standard configuration. Not accessible if PCI riser card field option is installed.

[4] Accepts low-profile PCIe card: height = 2.5 in., length = 6.6 in.

[5] Full-height PCI slots require installation of PCI riser card field option (full-height dimensions: height = 4.2 in., length = 6.875 in).

2.3 System Architecture

The systems covered in this guide feature an architecture based on the Intel Q45 Express chipset (Figure 2-2). All systems covered in this guide include the following key components:

- Intel Pentium Dual-Core, Core 2 Duo, Core 2 Quad, or Celeron processor.
- Intel Q45 Express chipset - Includes Q45 GMCH and 82801 ICH10-DO
- Super I/O (SIO) controller supporting PS/2 keyboard and mouse peripherals
- AD1884A audio controller supporting line in, line out, microphone in, and headphones out
- Intel 82567LM GbE network interface controller

The Q45 chipset provides a major portion of system functionality. Designed to complement the latest Intel processors, the Q45 GMCH integrates with the processor through a 800/1066/1333-MHz Front-Side Bus (FSB) and communicates with the ICH10-DO component through the Direct Media Interface (DMI). The integrated graphics controller of the Q45 on SFF and CMT systems can be upgraded through a PCI Express (PCIe) x16 graphics slot. All systems include a serial ATA (SATA) hard drive in the standard configuration.

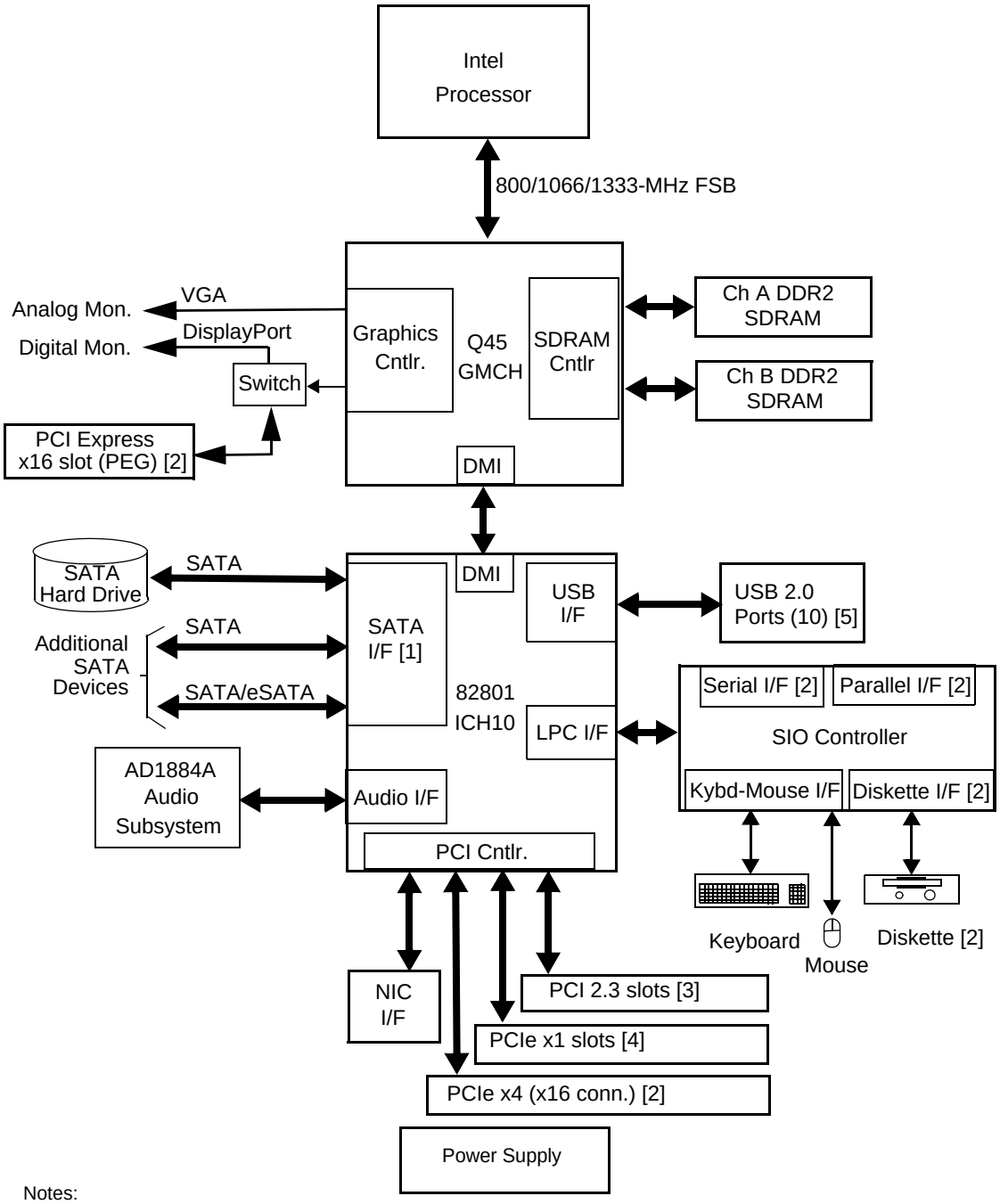
Table 2-2 lists the differences between models by form factor.

Table 2-2.
Architectural Differences By Form Factor

Function	USDT	SFF	CMT
Memory sockets	2 SODIMMs	4 DIMMs	4 DIMMs
PCIe 2.0 x16 graphics slot	No	1 [1]	1
PCIe x4 (x16 connector) graphics slot	No	1 [1]	1
# of PCIe 1.1 x1 slots	0	1 [1]	1
# of PCI 2.3 slots	0	1 [3]	3
Serial port	0	1 [4]	1 [4]
Parallel ports	0	optional	optonal
SATA interfaces	2	3	4
eSATA capability [2]	No	Yes	Yes

Notes:

[1] Low-profile slot. Not accessible if PCI riser is installed.
[2] Requires optional bracket/cable assembly.
[3] Low-profile slot in standard configuration. 2 full-height slots supported with optional PCI riser.
[4] 2nd serial port possible with optional adapter.



Notes:

[1] 2 SATA ports in USDT, 3 SATA ports in SFF, 4 SATA ports in CMT, and 1 eSATA port in SFF and CMT.
[2] SFF and CMT only
[3] 0 slots in USDT, 1 or 2 slots in SFF, 3 slots in CMT
[4] 1 MiniCard slot in USDT, 1 slot in SFF and CMT
[5] 8 ports accessible externally, 2 ports accessible internally

Figure 2-2. HP Compaq dc7900 Business PC Architecture, Block diagram

2.3.1 Intel Processor Support

The models covered in this guide are designed to support the following processor types:

- Intel Celeron: single- and dual-core performance
- Intel Pentium Dual-Core: Dual core performance
- Intel Core2 Duo: energy-efficient dual-core performance
- Intel Core2 Quad: energy efficient quad-core design

These processors are backward-compatible with software written for earlier x86 microprocessors and include streaming SIMD extensions (SSE, SSE2, and SSE3) for enhancing 3D graphics and speech processing performance. Intel processors with vPro Technology include hardware-based tools that allow corporate IT organizations to remotely manage and protect systems.

The system board includes a zero-insertion-force (ZIF) Socket-T designed for mounting an LGA775-type processor package.

CAUTION: The USDT form factor can support a processor rated up to 65 watts. The SFF and CMT form factors can support a processor rated up to 95 watts. Exceeding these limits can result in system damage and loss of data.

The processor heatsink/fan assembly mounting differs between form factors. Always use the same assembly or one of the same type when replacing the processor. Refer to the applicable Service Reference Guide for detailed removal and replacement procedures of the heatsink/fan assembly and the processor.

2.3.2 Chipset

The Intel Q45 Express chipset consists of a Graphics Memory Controller Hub (GMCH) and an enhanced I/O controller hub (ICH10-DO). Table 2-3 compares the functions provided by the chipsets.

Table 2-3
Chipset Components and Functionality

Components	Function
Q45 GMCH	Intel Graphics Media Accelerator 4500 (integrated graphics controller) PCIe 2.0 x16 graphics interface (1) SDRAM controller supporting unbuffered, non-ECC PC2-6400 DDR2 DIMMs or SODIMMs 800-, 1066-, or 1333-MHz FSB
82801 ICH10-DO	PCI 2.3 bus I/F PCI Express x1 LPC bus I/F SMBus I/F SATA I/F HD audio interface RTC/CMOS IRQ controller Power management logic USB 1.1/2.0 controllers supporting 12 ports (these systems provide 8 external, 3 internal) Gigabit Ethernet controller

The I/O controller hub (ICH10-DO) supports Intel vPro, which uses Active Management Technology (AMT). AMT is a hardware/firmware solution that operates on auxiliary power to allow 24/7 support of network alerting and management of the unit without regard to the power state or operating system. AMT capabilities include:

- System asset recovery (hardware and software configuration data)
- OS-independent system wellness and healing
- Software (virus) protection/management

2.3.3 Support Components

Input/output functions not provided by the chipset are handled by other support components. Some of these components also provide “housekeeping” and various other functions as well. Table 2-4 shows the functions provided by the support components.

Table 2-4
Support Component Functions

Component Name	Function
WPCD376H SIO Controller	Keyboard and pointing device I/F Diskette I/F [1] Serial I/F (COM1and COM2) [2] Parallel I/F (LPT1, LPT2, or LPT3) [3] PCI reset generation Interrupt (IRQ) serializer Power button and front panel LED logic GPIO ports Processor over temperature monitoring Fan control and monitoring Power supply voltage monitoring SMBus and Low Pin Count (LPC) bus I/F
Intel 82567LM Network Interface Controller	10/100/1000 Fast Ethernet network interface controller.
AD1884A HD Audio Codec	Audio mixer Two digital-to-analog stereo converters Two analog-to-digital stereo converters Analog I/O Supports stereo (two-channel) audio streams

NOTE:
[1] Not used in USDT form factor.
[2] Com1 supported only on SFF and CMT form factors. COM2 requires external bracket/cable assembly.
[3] Supported only on SFF and CMT form factors, requires external bracket/cable assembly.

2.3.4 System Memory

These systems implement a dual-channel Double Data Rate (DDR2) memory architecture. All models support DDR2 800- and 667-MHz DIMMs. The USDT system provides two SODIMM sockets supporting up to eight gigabytes of memory while the SFF and CMT form factors provide four DIMM sockets and support a total of 16 gigabytes of memory.

DDR and DDR2 DIMMs are NOT interchangeable.

SODIMM and DIMM components are NOT interchangeable.

2.3.5 Mass Storage

All models support at least two mass storage devices, with one being externally accessible for removable media. These systems provide the following interfaces for internal storage devices:

USDT: two SATA interfaces

SFF: three SATA interfaces and one eSATA port

CMT: four SATA interfaces and one eSATA port

These systems may be preconfigured or upgraded with a SATA hard drive and one removable media drive such as a CD-ROM drive.

2.3.6 Serial Interface

The SFF and CMT form factors include a serial port accessible at the rear of the chassis. The SFF and CMT form factors may be upgraded with a second serial port option. The serial interface is RS-232-C/16550-compatible and supports standard baud rates up to 115,200 as well as two high-speed baud rates of 230K and 460K.

2.3.7 Universal Serial Bus Interface

All models provide ten Universal Serial Bus (USB) ports. Two ports are accessible at the front of the unit, six ports are accessible on the rear panel, and two ports are accessible through a header on the system board. The SFF and CMT form factors support a media card reader module that connects to the internal header. These systems support USB 1.1 and 2.0 functionality on all ports.

BIOS Setup allows for the disabling of USB ports individually or in groups. In order to secure the system against a physical attack, ports may be disabled even if there is nothing physically connected to them, such as the two front ports for the media card reader module when the module is not present.

2.3.8 Network Interface Controller

All models feature an Intel gigabit Network Interface Controller (NIC) integrated on the system board. The controller provides automatic selection of 10BASE-T, 100BASE-TX, or 1000BASE-T operation with a local area network and includes power-down, wake-up, Alert-On-LAN (AOL), Alert Standard Format (ASF), and AMT features. An RJ-45 connector with status LEDs is provided on the rear panel.

2.3.9 Graphics Subsystem

These systems use the Q45 GMCH component, which includes an integrated graphics controller that can drive both an external VGA monitor and a DisplayPort digital display. The controller implements Dynamic Video Memory Technology (DVMT 3.0) for video memory. Table 2-5 lists the key features of the integrated graphics subsystem.

Table 2-5
Integrated Graphics Subsystem Statistics

	Q45 GMCH Integrated Graphics Controller
Recommended for	Hi 2D, Entry 3D
Bus Type	Int. PCI Express
Memory Amount	32 MB pre-allocated
Memory Type	DVMT 3.0
DAC Speed	400 MHz
Maximum 2D Resolution	2048x1536 @ 85 Hz
Hardware Acceleration	Quick Draw, DirectX 9, Direct Draw, Direct Show, Open GL 1.45, MPEG 1-2, Indeo
Outputs	1 VGA, 1 DisplayPort 1.1 [see text]

All systems include a legacy VGA connector and a DisplayPort connector and support dual monitor operation. The DisplayPort includes a multimode feature that allows a DVI or VGA adapter to be connected to the DisplayPort.

These systems also include two PCIe graphics slots (one x16, one x4/x16 connector) to ensure full graphics upgrade capabilities.

2.3.10 Audio Subsystem

These systems use the integrated High Definition audio controller of the chipset and the ADI AD1884A High Definition audio codec. HD audio provides enhanced audio performance with higher sampling rates, refined signal interfaces, and audio processors with increased signal-to-noise ratio. The audio line input jack can be re-configured as a microphone input, and multi-streaming is supported. These systems include a 1.5-watt output amplifier driving an internal speaker, which can be muted with the F10 BIOS control. All models include front panel-accessible stereo microphone input and headphone output audio jacks.

2.4 Specifications

This section includes the environmental, electrical, and physical specifications for the systems covered in this guide. Where provided, metric statistics are given in parenthesis. Specifications are subject to change without notice.

Table 2-6
Environmental Specifications (Factory Configuration)

Parameter	Operating	Non-operating
Ambient Air Temperature	50° to 95° F (10° to 35° C, max. rate of change ≤ 10°C/Hr)	-22° to 140° F (-30° to 60° C, max. rate of change ≤ 20°C/Hr)
Shock (w/o damage)	5 Gs [1]	20 Gs [1]
Vibration	0.000215 G^2/Hz, 10-300 Hz	0.0005 G^2/Hz, 10-500 Hz
Humidity	10-90% Rh @ 28° C max. wet bulb temperature	5-95% Rh @ 38.7° C max. wet bulb temperature
Maximum Altitude	10,000 ft (3048 m) [2]	30,000 ft (9144 m) [2]

NOTE:
[1] Peak input acceleration during an 11 ms half-sine shock pulse.
[2] Maximum rate of change: 1500 ft/min.

Table 2-7
Power Supply Electrical Specifications

Parameter	Value
Input Line Voltage:	
Nominal:	100–240 VAC
Maximum	90–264 VAC
Input Line Frequency Range:	
Nominal	50–60 Hz
Maximum	47–63 Hz
Energy Star 4.0 with 80Plus Bronze-level compliancy	
USDT	Standard
SFF & CMT	Optional
Maximum Continuous Power:	
USDT	135 watts
SFF	240 watts
CMT	365 watts

NOTE:
Energy Star 4.0 with 80Plus Bronze-level compliancy option available for SFF and CMT form factors.

Table 2-8
Physical Specifications

Parameter	USDT [2]	SFF [2]	CMT [3]
Height	2.60 in (6.60 cm)	3.95 in (10.03 cm)	17.63 in (44.8 cm)
Width	9.90 in (25.15 cm)	13.3 in (33.78 cm)	7.0 in (16.8 cm)
Depth	10.0 in (25.40 cm)	14.9 in (37.85 cm)	17.8 in (45.21 cm)
Weight [1]	7.0 lb (3.18 kg)	18.75 lb (8.50 kg)	26.2 lb (11.89 kg)
Load-bearing ability of chassis [4]	77.1 lb (35 kg)	77.1 lb (35 kg)	77.1 lb (35 kg)

NOTES:

[1] System configured with 1 hard drive, 1 diskette drive (SFF and CMT only), and no PCI cards.

[2] Desktop (horizontal) configuration.

[3] Minitower configuration. For desktop configuration, swap Height and Width dimensions.

[4] Applicable to unit in desktop orientation only and assumes reasonable type of load such as a monitor.

Table 2-9
Optical Drive Specifications

Parameter	DVD-ROM	CD-RW/DVD-ROM Combo	HP SuperMulti LightScribe Combo
Interface Type	SATA [1]	SATA [1]	SATA [1]
Max. read/write speeds by media type	DVD-RAM: 4x/na DVD+RW: 8x/na DVD-RW: 8x/na DVD+R DL: 8x/na DVD-R DL: 8x/na DVD-ROM: 16x/na DVD+R: 8x/na DVD-R: 8x/na CD-ROM: 48x/na CD-RW: 32x/na CD-R: 48x/na	DVD-RAM: 12x/12x DVD+RW: 8x/8x DVD-RW: 8x/6x DVD+R DL: 8x/8x DVD-R DL: 8x/8x DVD-ROM: 16x/na DVD-ROM DL: 8x/na DVD+R: 16x/16x DVD-R: 16x/16x CD-ROM: 48x/na CD-RW: 32x/32x CD-R: 48x/48x	DVD-RAM: 12x/12x DVD+RW: 8x/8x DVD-RW: 8x/6x DVD+R DL: 8x/8x DVD-R DL: 8x/8x DVD-ROM: 16x/na DVD-ROM DL: 8x/na DVD+R: 16x/16x DVD-R: 16x/16x CD-ROM: 48x/na CD-RW: 32x/32x CD-R: 48x/48x
Maximum Transfer Rate (Reads)	DVD:, 21.6 KB/s; CD: 7.2 KB/s	DVD:, 21.6 KB/s; CD: 7.2 KB/s	DVD:, 21.6 KB/s; CD: 7.2 KB/s
Media Capacity (DVD)	DL: 8.5 GB, Std: 4.7 GB	DL: 8.5 GB, Std: 4.7 GB	DL: 8.5 GB, Std: 4.7 GB
Average Access Time: Random Full Stroke	DVD: <140 ms, CD: <125 ms DVD: <250 ms, CD: <210 ms	DVD: <140 ms, CD: <125 ms DVD: <250 ms, CD: <210 ms	DVD: <140 ms, CD: <125 ms DVD: <250 ms, CD: <210 ms
Media lable creation?	No	No	Yes [2]

NOTE
[1] USDT models use “slim” drive.
[2] Requires special label-etchable media.

Table 2-10
Hard Drive Specifications

Parameter	80 GB	160 GB	250 GB [4]
Drive Size	2.5 & 3.5 in.[1]	2.5 & 3.5 in [1]	3.5 in
Interface	SATA	SATA	SATA
Transfer Rate	1.5 & 3.0 Gb/s [2]	1.5 & 3.0 Gb/s [2]	3.0 Gb/s
Drive Protection System Support?	Yes	Yes	Yes
Typical Seek Time (w/settling)			
Single Track	0.8 ms	0.8 ms	1.0 ms
Average	9 ms	9 ms	11 ms
Full Stroke	17 ms	17 ms	18 ms
Disk Format (logical blocks)	156,301,488	320,173,056	488,397,168
Rotation Speed	5400/7200/ 10K RPM [3]	5400/7200/ 10K RPM [3]	7200 RPM
Drive Fault Prediction	SMART IV	SMART IV	SMART IV

NOTES:

[1] USDT supports 2.5-in. drives only.

[2] USDT supports 1.5 Gb/s drives only.

[3] USDT supports up to 7200-RPM drives only.

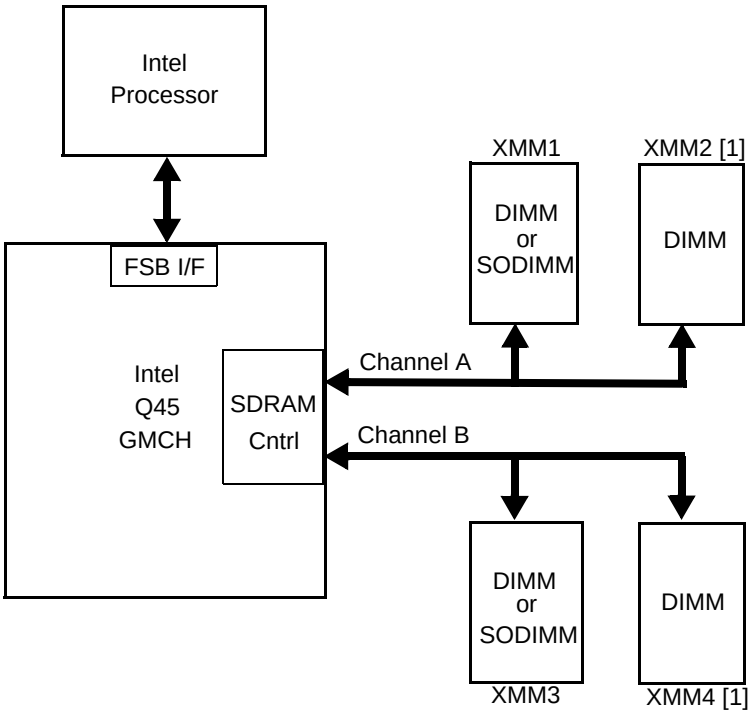
[4] Supported by SFF and CMT form factors only.

3

Processor/Memory Subsystem

3.1 Introduction

This systems support the Intel Pentium and Core processor families and use the Q45 chipset (Figure 3-1). These systems support PC2-6400 and PC2-5300 DDR2 memory modules. This chapter describes the processor/memory subsystem.



Note:
[1] Not present on USDT form factor.

Figure 3-1. Processor/Memory Subsystem Architecture

This chapter includes the following topics:

- Intel processor (3.2)
- Memory subsystem (3.3)

3.2 Intel Processors

These systems each feature an Intel processor in a FC-LGA775 package mounted with a heat sink in a zero-insertion force socket. The mounting socket allows the processor to be easily changed for upgrading.

3.2.1 Intel Processor Overview

The models covered in this guide support Intel Celeron, Pentium, and Core 2 processors, including the latest Intel Core 2 Duo, and Core 2 Quad processors.

Key features of supported Intel processors include:

- Dual- or quad-core architecture—Provides full parallel processing.
- Execution Trace Cache— A new feature supporting the branch prediction mechanism, the trace cache stores translated sequences of branching micro-operations (ops) and is checked when suspected re-occurring branches are detected in the main processing loop. This feature allows instruction decoding to be removed from the main processing loop.
- Rapid Execution Engine—Arithmetic Logic Units (ALUs) run at twice (2x) processing frequency for higher throughput and reduced latency.
- Up to 12-MB of L2 cache—Using a 32-byte-wide interface at processing speed, the large L2 cache provides a substantial increase.
- Advanced dynamic execution—Using a larger (4K) branch target buffer and improved prediction algorithm, branch mis-predictions are significantly reduced
- Additional Streaming SIMD extensions (SSE2 and SSE3)—In addition to the SSE support provided by earlier processors, the latest processors include additional MMX instructions that enhance:
  - Streaming video/audio processing
  - Photo/video editing
  - Speech recognition
  - 3D processing
  - Encryption processing
- Quad-pumped Front Side Bus (FSB)—The FSB uses a 200-MHz clock for qualifying the buses' control signals. However, address information is transferred using a 2x strobe while data is transferred with a 4x strobe, providing a maximum data transfer rate that is four times that of earlier processors.

The Intel processor increases processing speed by using higher clock speeds with hyper-pipelined technology, therefore handling significantly more instructions at a time. The Arithmetic Logic Units (ALUs) of all processors listed above run at twice the core speed.

3.2.2 Processor Changing/Upgrading

All models use the LGA775 ZIF (Socket T) mounting socket. These systems require that the processor use an integrated heatsink/fan assembly. A replacement processor must use the same type heatsink/fan assembly as the original to ensure proper cooling. The heatsink and attachment clip are specially designed provide maximum heat transfer from the processor component.

CAUTION: Attachment of the heatsink to the processor is critical on these systems. Improper attachment of the heatsink will likely result in a thermal condition. Although the system is designed to detect thermal conditions and automatically shut down, such a condition could still result in damage to the processor component. Refer to the applicable Service Reference Guide for processor installation instructions.

Table 3-1 provides a sample listing of processors supported by these systems.

Table 3-1
Supported Processors (partial listing)

Intel Model	Core design	Features	Clock Speed in GHz	FSB Speed in MHz	L2 Cache	Form Factor support
Q6700	quad	VT, [1]	2.66	1066	8 MB	SFF, CMT
Q6600	quad	VT, [1]	2.40	1066	8 MB	SFF, CMT
E6850	dual	vPro, VT, TXT, [1]	3.00	1333	4 MB	all
E6750	dual	vPro, VT, TXT, [1]	2.66	1333	4 MB	all
E6550	dual	vPro, VT, TXT, [1]	2.33	1333	4 MB	all
E4500	dual	[1]	2.20	800	2 MB	all
E4400	dual	[1]	2.00	800	2 MB	all
E2180	dual	[1]	2.00	800	1 MB	all
E2160	dual	[1]	1.80	800	1 MB	all
440	single	[1]	2.00	800	512 KB	all

NOTE:
[1] Standard Intel feature set including EM64T, XD, and EIST support. Refer to www.intel.com for detailed information.

CAUTION: The USDT form factor can support a processor with a maximum power consumption of 65 watts. The SFF and CMT form factors can support a processor with a maximum power consumption of 95 watts. Exceeding these limits can result in system damage and lost data.

3.3 Memory Subsystem

All models support non-ECC PC2-5300 and PC2-6400 DDR2 memory. The USDT form factor supports up to eight gigabytes of memory while the SFF and CMT form factors support up to 16 gigabytes of memory.

The DDR SDRAM "PCxxxx" reference designates bus bandwidth (i.e., a PC2-5300 module can, operating at a 667-MHz effective speed, provide a throughput of 5300 MBps (8 bytes × 667MHz)). Memory speed types may be mixed within a system, although the system BIOS will set the memory controller to work at speed of the slowest memory module.

The USDT system board provides two SODIMM sockets and the SFF and CMT system boards provide four DIMM sockets

- XMM1, channel A (black)
- XMM2, channel A (white, not present in USDT form factor)
- XMM3, channel B (white)
- XMM4, channel B (white, not present in USDT form factor)

Memory modules do not need to be installed in pairs although installation of pairs (especially matched sets) provides the best performance. The XMM1 socket must be populated for proper support of Intel Active Management Technology (AMT). The BIOS will detect the module population and set the system accordingly as follows:

- Single-channel mode - memory installed for one channel only
- Dual-channel asymetric mode - memory installed for both channels but of unequal channel capacities.
- Dual-channel interleaved mode (recommended) - memory installed for both channels and offering equal channel capacities, proving the highest performance.

These systems support memory modules with the following parameters:

- Unbuffered, compatible with SPD rev. 1.0
- 512-Mb, and 1-Gb memory technologies for x8 and x16 devices
- CAS latency (CL) of 5 or 6 (depending on memory speed)
- Single or double-sided
- Non-ECC memory only

The SPD format supported by these systems complies with the JEDEC specification for 128-byte EEPROMs. This system also provides support for 256-byte EEPROMs to include additional HP-added features such as part number and serial number.

If BIOS detects an unsupported memory module, a "**memory incompatible**" message will be displayed and the system will halt. **These systems are shipped with non-ECC modules only**.

An installed mix of memory module types is acceptable but operation will be constrained to the level of the module with the lowest (slowest) performance.

If an incompatible memory module is detected the NUM LOCK will blink for a short period of time during POST and an error message may or may not be displayed before the system hangs.

3.3.1 Memory Upgrading

Table 3-2 shows suggested memory configurations for these systems. Note that the USDT form factor provides only two memory sockets.

Table 3-2 does not list all possible configurations.

Table 3-2.
Memory Socket Loading [1]

Channel A		Channel B		
Socket 1	**Socket 2 [2]**	**Socket 3**	**Socket 4 [2]**	**Total**
512 MB	none	none	none	512-MB
512 MB	none	512 MB	none	1-GB [3]
1-GB	none	none	none	1-GB
1 GB	none	1 GB	none	2 GB [3]
1 GB	1 GB	1 GB	1 GB	4-GB [3]
2 GB	none	2 GB	none	4-GB [3]
4 GB	4 GB	4 GB	4 GB	16-GB [3, 4]

NOTE:

[1] USDT form factor uses SODIMM sockets. SFF and CMT form factors use DIMM sockets.

[2] Not present on USDT form factor.

[3] Dual-channel symetrical

[4] Only SFF and CMT support this size memory

HP recommends using symmetrical loading (same-capacity, same-speed modules across both channels) to achieve the best performance.

CAUTION: Always power down the system and disconnect the power cord from the AC outlet before adding or replacing memory modules. Changing memory modules while the unit is plugged into an active AC outlet could result in equipment damage.

Memory amounts over 3 GB may not be fully accessible with 32-bit operating systems due to system resource requirements. Addressing memory above 4 GB requires a 64-bit operating system.

3.3.2 Memory Mapping and Pre-allocation

Figure 3-2 shows the system memory map. The Q45 Express chipset includes a Management Engine that pre-allocates a portion of system memory (16 MB for one module, 32 MB for two modules) for managment functions. In addition, the internal graphics controller pre-allocates a portion of system memory for video use (refer to chapter 6). Pre-allocated memory is not available to the operating system. The amount of system memory reported by the OS will be the total amount installed less the pre-allocated amount.

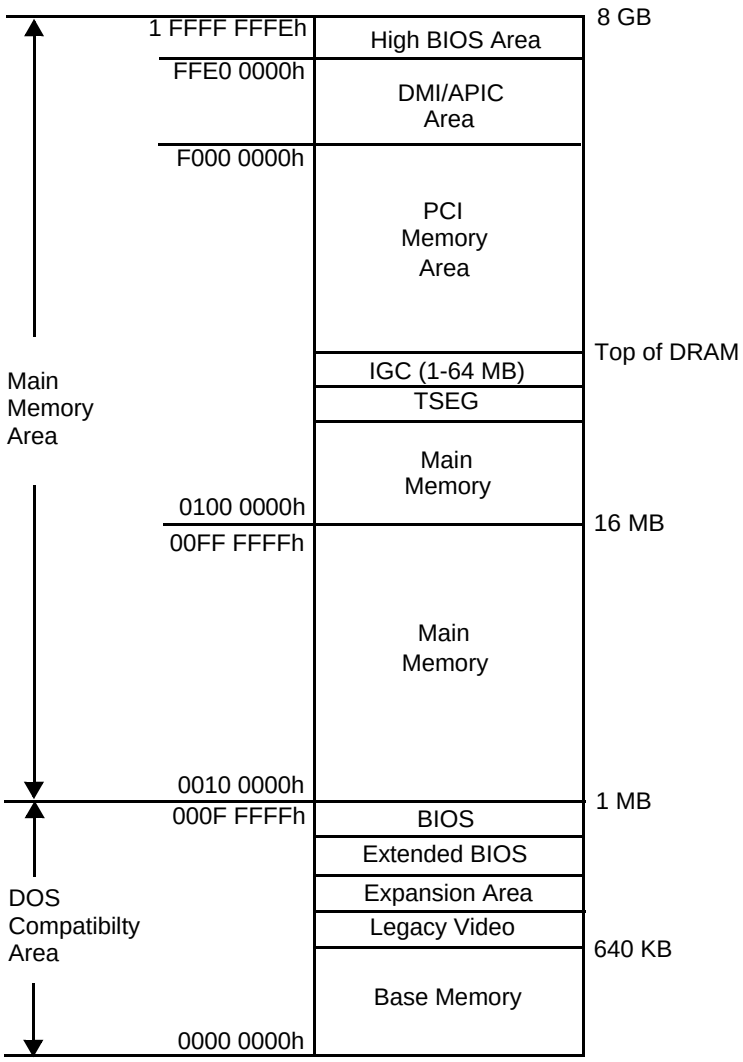


Figure 3-2. System Memory Map (for maximum of 8 gigabytes)

All locations in memory are cacheable. Base memory is always mapped to DRAM. The next 128 KB fixed memory area can, through the north bridge, be mapped to DRAM or to PCI space. Graphics RAM area is mapped to PCI locations.

4

System Support

4.1 Introduction

This chapter covers subjects dealing ICH10 with basic system architecture and covers the following topics:

- PCI bus overview (4.2)
- System resources (4.3)
- Real-time clock and configuration memory (4.4)
- System management (4.5)
- Register map and miscellaneous functions (4.6)

This chapter covers functions provided by off-the-shelf chipsets and therefore describes only basic aspects of these functions as well as information unique to the systems covered in this guide. For detailed information on specific components, refer to the applicable manufacturer's documentation.

4.2 PCI Bus Overview

This section describes the PCI bus in general and highlights bus implementation for systems covered in this guide. For detailed information regarding PCI bus operation, refer to the appropriate PCI specification or the PCI web site: www.pcisig.com.

These systems implement the following types of PCI buses:

- PCI 2.3 - Legacy parallel interface operating at 33-MHz
- PCI Express - High-performance interface capable of using multiple TX/RX high-speed lanes of serial data streams

4.2.1 PCI 2.3 Bus Operation

The PCI 2.3 bus consists of a 32-bit path (AD31-00 lines) that uses a multiplexed scheme for handling both address and data transfers. A bus transaction consists of an address cycle and one or more data cycles, with each cycle requiring a clock (PCICLK) cycle. High performance is achieved during burst modes in which a transaction with contiguous memory locations requires that only one address cycle be conducted and subsequent data cycles are completed using auto-incremented addressing.

Devices on the PCI bus must comply with PCI protocol that allows configuration of that device by software. In this system, configuration mechanism #1 (as described in the PCI Local Bus specification Rev. 2.3) is employed.

Table 4-1 shows the standard configuration of device numbers and IDSEL connections for components and slots residing on a PCI 2.3 bus.

Table 4-1
PCI Component Configuration Access

PCI Component	Notes	Function #	Device #	PCI Bus #	IDSEL Wired to:
Q45 GMCH:					--
Host/DMI Bridge		0	28	0	
Host/PCI Expr. Bridge		0	1	0	
Integrated Graphics Cntlr.		0	2	0	
PCI Express x16 graphics slot		0	0	1	--
82801 ICH10					--
PCI Bridge		0	30	0	
LPC Bridge		0	31	0	
SATA Controller #1		2	31	0	
SMBus Controller		3	31	0	
SATA/eSATA Controller #2	[5]	5	31	0	
Thermal System		6	31	0	
USB 1.1 Controller #1		0	29	0	
USB 1.1 Controller #2		1	29	0	
USB 1.1 Controller #3		2	29	0	
USB 1.1 Controller #4		0	26	0	
USB 1.1 Controller #5		1	26	0	
USB 1.1 Controller #6		3 [2]	29 [2]		
USB 2.0 Controller #1		7	29	0	
USB 2.0 Controller #2		7	26	0	
GbE NIC		0	25	0	
Intel HD audio controller		0	27	0	
PCIe port 1	[3]	0	28	0	
PCIe port 2	[1]	1	28	0	
PCIe port 3	[1]	2	28	0	
PCIe port 4	[1]	3	28	0	
PCIe port 5		4	28	0	
PCIe port 6		5	28	0	
PCI 2.3 slot 1	[3]	0	4	7	AD20
PCI 2.3 slot 2	[3]	0	11	7	AD25
PCI 2.3 slot 3	[4]	0	10	7	AD27
PCIe x1 slot 1	[3]	0	0	32	
PCIe x1 slot 2	[3]	0	0	48	

NOTES:
[1] Function not used in these systems.
[2] USB 1.1 controllers in 6+6 configuration. 8+4 configuration will have USB 1.1 controller #6 use Function 26, Device 2.
[3] SFF and CMT form factors only.
[4] CMT form factor only
[5] Function is only visible in IDE mode (not visible in AHCI orRAID SATA emulation mode).

The PCI bus supports a bus master/target arbitration scheme. A bus master is a device that has been granted control of the bus for the purpose of initiating a transaction. A target is a device that is the recipient of a transaction. The Request (REQ), Grant (GNT), and FRAME signals are used by PCI bus masters for gaining access to the PCI bus. When a PCI device needs access to the PCI bus (and does not already own it), the PCI device asserts its REQn signal to the PCI bus arbiter (a function of the system controller component). If the bus is available, the arbiter asserts the GNTn signal to the requesting device, which then asserts FRAME and conducts the address phase of the transaction with a target. If the PCI device already owns the bus, a request is not needed and the device can simply assert FRAME and conduct the transaction. Table 4-2 shows the grant and request signals assignments for the devices on the PCI bus.

Table 4-2.
PCI Bus Mastering Devices

Device	REQ/GNT Line	Note
PCI Connector Slot 1	REQ0/GNT0	[1]
PCI Connector Slot 2	REQ1/GNT1	[1]
PCI Connector Slot 3	REQ2/GNT2	[2]

NOTE:

[1] SFF and CMT form factors only.

[2] CMT form factor only

PCI bus arbitration is based on a round-robin scheme that complies with the fairness algorithm specified by the PCI specification. The bus parking policy allows for the current PCI bus owner (excepting the PCI/ISA bridge) to maintain ownership of the bus as long as no request is asserted by another agent. Note that most CPU-to-DRAM accesses can occur concurrently with PCI traffic, therefore reducing the need for the Host/PCI bridge to compete for PCI bus ownership.

4.2.2 PCI Express Bus Operation

The PCI Express (PCIe) v1.1 bus is a high-performace extension of the legacy PCI bus specification. The PCI Express bus uses the following layers:

- Software/driver layer
- Transaction protocol layer
- Link layer
- Physical layer

Software/Driver Layer

The PCI Express bus maintains software compatibility with PCI 2.3 and earlier versions so that there is no impact on existing operating systems and drivers. During system intialization, the PCI Express bus uses the same methods of device discovery and resource allocation that legacy PCI-based operating systems and drivers are designed to use.

Transaction Protocol Layer

The transaction protocol layer processes read and write requests from the software/driver layer and generates request packets for the link layer. Each packet includes an identifier allowing any required responcse packets to be directed to the originator.

Link Layer

The link layer provides data integrity by adding a sequence information prefix and a CRC suffix to the packet created by the transaction layer. Flow-control methods ensure that a packet will only be transferred if the receiving device is ready to accomodate it. A corrupted packet will be automatically re-sent.

Physical Layer

The PCI Express bus uses a point-to-point, high-speed TX/RX serial lane topology. One or more full-duplex lanes transfer data serially, and the design allows for scalability depending on end-point capabilities. Each lane consists of two differential pairs of signal paths; one for transmit, one for receive (Figure 4-1).

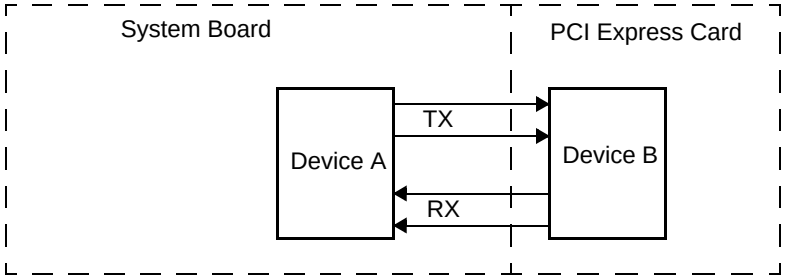


Figure 4-1. PCI Express Bus Lane

Each byte is transferred using 8b/10b encoding. which embeds the clock signal with the data. Operating at a 2.5 Gigabit transfer rate, a single lane can provide a data flow of 200 MBps. The bandwidth is increased if additional lanes are available for use. During the initialization process, two PCI Express devices will negotiate for the number of lanes available and the speed the link can operate at. In a x1 (single lane) interface, all data bytes are transferred serially over the lane. In a multi-lane interface, data bytes are distributed across the lanes using a multiplex scheme.

4.2.3 Option ROM Mapping

During POST, the PCI bus is scanned for devices that contain their own specific firmware in ROM. Such option ROM data, if detected, is loaded into system memory's DOS compatibility area (refer to the system memory map shown in chapter 3).

4.2.4 PCI Interrupts

Eight interrupt signals (INTA- thru INTH-) are available for use by PCI devices. These signals may be generated by on-board PCI devices or by devices installed in the PCI slots. For more information on interrupts including PCI interrupt mapping refer to the “System Resources” section 4.3.

4.2.5 PCI Power Management Support

This system complies with the PCI Power Management Interface Specification (rev 1.0). The PCI Power Management Enable (PME-) signal is supported by the chipset and allows compliant PCI peripherals to initiate the power management routine.

4.2.6 PCI Connectors

PCI 2.3 Connector

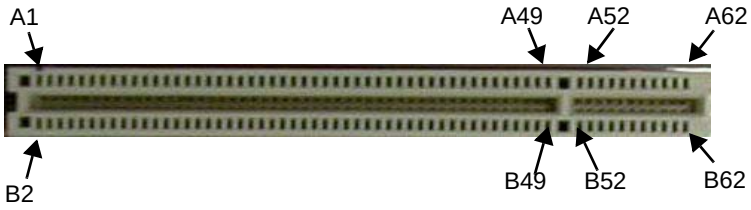


Figure 4-2. 32-bit, 5.0-volt PCI 2.3 Bus Connector

Table 4-3.
PCI 2.3 Bus Connector Pinout

Pin	B Signal	A Signal	Pin	B Signal	A Signal	Pin	B Signal	A Signal
01	-12 VDC	TRST-	22	GND	AD28	43	+3.3 VDC	PAR
02	TCK	+12 VDC	23	AD27	AD26	44	C/BE1-	AD15
03	GND	TMS	24	AD25	GND	45	AD14	+3.3 VDC
04	TDO	TDI	25	+3.3 VDC	AD24	46	GND	AD13
05	+5 VDC	+5 VDC	26	C/BE3-	IDSEL	47	AD12	AD11
06	+5 VDC	INTA-	27	AD23	+3.3 VDC	48	AD10	GND
07	INTB-	INTC-	28	GND	AD22	49	GND	AD09
08	INTD-	+5 VDC	29	AD21	AD20	50	Key	Key
09	PRSNT1-	Reserved	30	AD19	GND	51	Key	Key
10	RSVD	+5 VDC	31	+3.3 VDC	AD18	52	AD08	C/BE0-
11	PRSNT2-	Reserved	32	AD17	AD16	53	AD07	+3.3 VDC
12	GND	GND	33	C/BE2-	+3.3 VDC	54	+3.3 VDC	AD06
13	GND	GND	34	GND	FRAME-	55	AD05	AD04
14	RSVD	+3.3 AUX	35	IRDY-	GND	56	AD03	GND
15	GND	RST-	36	+3.3 VDC	TRDY-	57	GND	AD02
16	CLK	+5 VDC	37	DEVSEL-	GND	58	AD01	AD00
17	GND	GNT-	38	GND	STOP-	59	+5 VDC	+5 VDC
18	REQ-	GND	39	LOCK-	+3.3 VDC	60	ACK64-	REQ64-
19	+5 VDC	PME-	40	PERR-	SDONE n	61	+5 VDC	+5 VDC
20	AD31	AD30	41	+3.3 VDC	SBO-	62	+5 VDC	+5 VDC
21	AD29	+3.3 VDC	42	SERR-	GND			

PCI Express Connectors

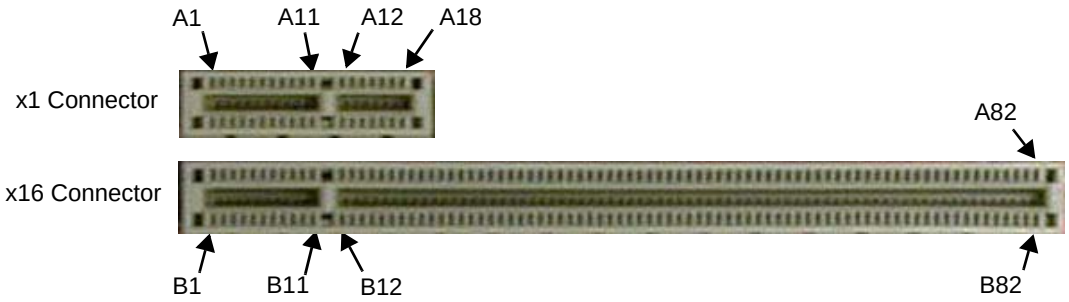


Figure 4-3. PCI Express Bus Connectors

Table 4-4.
PCI Express Bus Connector Pinout

Pin	B Signal	A Signal	Pin	B Signal	A Signal	Pin	B Signal	A Signal
01	+12 VDC	PRSNT1#	29	GND	PERp3	57	GND	PERn9
02	+12 VDC	+12 VDC	30	RSVD	PERn3	58	PETp10	GND
03	RSVD	+12 VDC	31	PRSNT2#	GND	59	PETn10	GND
04	GND	GND	32	GND	RSVD	60	GND	PERp10
05	SMCLK	+5 VDC	33	PETp4	RSVD	61	GND	PERn10
06	+5 VDC	JTAG2	34	PETn4	GND	62	PETp11	GND
07	GND	JTAG4	35	GND	PERp4	63	PETn11	GND
08	+3.3 VDC	JTAG5	36	GND	PERn4	64	GND	PERp11
09	JTAG1	+3.3 VDC	37	PETp5	GND	65	GND	PERn11
10	3.3 Vaux	+3.3 VDC	38	PETn5	GND	66	PETp12	GND
11	WAKE	PERST#	39	GND	PERp5	67	PETn12	GND
12	RSVD	GND	40	GND	PERn5	68	GND	PERp12
13	GND	REFCLK+	41	PETp6	GND	69	GND	PERn12
14	PETp0	REFCLK-	42	PETn6	GND	70	PETp13	GND
15	PETn0	GND	43	GND	PERp6	71	PETn13	GND
16	GND	PERp0	44	GND	PERn6	72	GND	PERp13
17	PRSNT2#	PERn0	45	PETp7	GND	73	GND	PERn13
18	GND	GND	46	PETn7	GND	74	PETp14	GND
19	PETp1	RSVD	47	GND	PERp7	75	PETn14	GND
20	PETn1	GND	48	PRSNT2#	PERn7	76	GND	PERp14
21	GND	PERp1	49	GND	GND	77	GND	PERn14
22	GND	PERn1	50	PETp8	RSVD	78	PETp15	GND
23	PETp2	GND	51	PETn8	GND	79	PETn15	GND
24	PETn2	GND	52	GND	PERp8	80	GND	PERp15
25	GND	PERp2	53	GND	PERn8	81	PRSNT2#	PERn15
26	GND	PERn2	54	PETp9	GND	82	RSVD	GND
27	PETp3	GND	55	PETn9	GND			
28	PETn3	GND	56	GND	PERp9			

4.3 System Resources

This section describes the availability and basic control of major subsystems, otherwise known as resource allocation or simply “system resources.” System resources are provided on a priority basis through hardware interrupts and DMA requests and grants.

4.3.1 Interrupts

The microprocessor uses two types of hardware interrupts; maskable and nonmaskable. A maskable interrupt can be enabled or disabled within the microprocessor by the use of the STI and CLI instructions. A nonmaskable interrupt cannot be masked off within the microprocessor, but may be inhibited by legacy hardware or software means external to the microprocessor.

The maskable interrupt is a hardware-generated signal used by peripheral functions within the system to get the attention of the microprocessor. Peripheral functions produce a unique INTA-H (PCI) or IRQ0-15 (ISA) signal that is routed to interrupt processing logic that asserts the interrupt (INTR-) input to the microprocessor. The microprocessor halts execution to determine the source of the interrupt and then services the peripheral as appropriate.

Most IRQs are routed through the I/O controller of the super I/O component, which provides the serializing function. A serialized interrupt stream is then routed to the ICH component.

Interrupts may be processed in one of two modes (selectable through the F10 Setup utility):

- 8259 mode
- APIC mode

These modes are described in the following subsections.

8259 Mode

The 8259 mode handles interrupts IRQ0-IRQ15 in the legacy (AT-system) method using 8259-equivalent logic. If more than one interrupt is pending, the highest priority (lowest number) is processed first.

APIC Mode

The Advanced Programmable Interrupt Controller (APIC) mode provides enhanced interrupt processing with the following advantages:

- Eliminates the processor's interrupt acknowledge cycle by using a separate (APIC) bus
- Programmable interrupt priority
- Additional interrupts (total of 24)

The APIC mode accommodates eight PCI interrupt signals (PIRQA-..PIRQH-) for use by PCI devices. The PCI interrupts are evenly distributed to minimize latency and wired as shown in Table 4-5.

Table 4-5.
PCI Interrupt Distribution

	System Interrupts							
System Board Connector	**PIRQ A**	**PIRQ B**	**PIRQ C**	**PIRQ D**	**PIRQ E**	**PIRQ F**	**PIRQ G**	**PIRQ H**
PCI slot 1 (J20) [1]					A	B	C	D
PCI slot 2 (J21) [1]					D	A	B	C
PCI slot 3 (J22) [2]					C	D	A	B

NOTES:

[1] SFF and CMT only
[2] CMT only

The PCI interrupts can be configured by PCI Configuration Registers 60h..63h to share the standard ISA interrupts (IRQn).

The APIC mode is supported by Windows NT, Windows 2000, and Windows XP, and Windows Vista operating systems. Systems running the Windows 95 or 98 operating system will need to run in 8259 mode.

4.3.2 Direct Memory Access

Direct Memory Access (DMA) is a method by which a device accesses system memory without involving the microprocessor. Although the DMA method has been traditionally used to transfer blocks of data to or from an ISA I/O device, PCI devices may also use DMA operation as well. The DMA method reduces the amount of CPU interactions with memory, freeing the CPU for other processing tasks. For detailed information regarding DMA operation, refer to the data manual for the Intel 82801 ICH10 I/O Controller Hub.

4.4 Real-Time Clock and Configuration Memory

The Real-time clock (RTC) and configuration memory (also referred to as "CMOS") functions are provided by the 82801 component and is MC146818-compatible. As shown in the following figure, the 82801 ICH10 component provides 256 bytes of battery-backed RAM divided into two 128-byte configuration memory areas. The RTC uses the first 14 bytes (00-0Dh) of the standard memory area. All locations of the standard memory area (00-7Fh) can be directly accessed using conventional OUT and IN assembly language instructions through I/O ports 70h/71h, although the suggested method is to use the INT15 AX=E823h BIOS call.

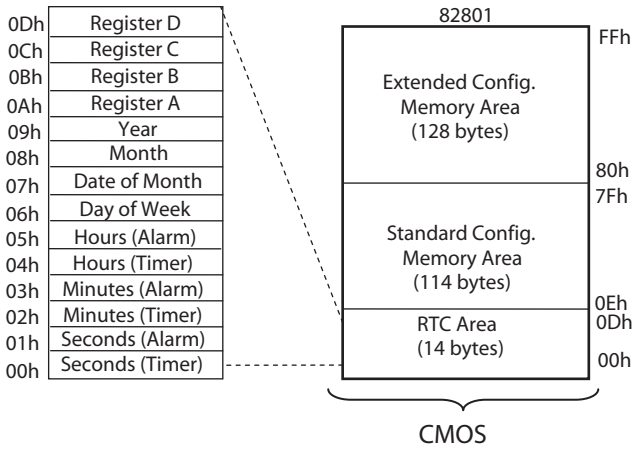


Figure 4 4. Configuration Memory Map

A lithium 3-VDC battery is used for maintaining the RTC and configuration memory while the system is powered down. During system operation a wire-Ored circuit allows the RTC and configuration memory to draw power from the power supply. The battery is located in a battery holder on the system board and has a life expectancy of three or more years. When the battery has expired it is replaced with a CR2032 or equivalent 3-VDC lithium battery.

4.4.1 Clearing CMOS

The contents of configuration memory (including the Power-On Password) can be cleared by the following procedure:

1. Turn off the unit.
2. Disconnect the AC power cord from the outlet and/or system unit.
3. Remove the chassis hood (cover) and insure that no LEDs on the system board are illuminated.
4. On the system board, press and hold the CMOS clear button (switch SW50, colored yellow) for at least 5 seconds.
5. Replace the chassis hood (cover).
6. Reconnect the AC power cord to the outlet and/or system unit.
7. Turn the unit on.

To clear only the Power-On Password refer to section 4.5.1.

4.4.2 Standard CMOS Locations

Table 4-6 describes standard configuration memory locations 0Ah-3Fh. These locations are accessible through using OUT/IN assembly language instructions using port 70/71h or BIOS function INT15, AX=E823h.

Table 4-6.
Configuration Memory (CMOS) Map

Location	Function	Location	Function
00-0Dh	Real-time clock	24h	System board ID
0Eh	Diagnostic status	25h	System architecture data
0Fh	System reset code	26h	Auxiliary peripheral configuration
10h	Diskette drive type	27h	Speed control external drive
11h	Reserved	28h	Expanded/base mem. size, IRQ12
12h	Hard drive type	29h	Miscellaneous configuration
13h	Security functions	2Ah	Hard drive timeout
14h	Equipment installed	2Bh	System inactivity timeout
15h	Base memory size, low byte/KB	2Ch	Monitor timeout, Num Lock Cntrl
16h	Base memory size, high byte/KB	2Dh	Additional flags
17h	Extended memory, low byte/KB	2Eh-2Fh	Checksum of locations 10h-2Dh
18h	Extended memory, high byte/KB	30h-31h	Total extended memory tested
19h	Hard drive 1, primary controller	32h	Century
1Ah	Hard drive 2, primary controller	33h	Miscellaneous flags set by BIOS
1Bh	Hard drive 1, secondary controller	34h	International language
1Ch	Hard drive 2, secondary controller	35h	APM status flags
1Dh	Enhanced hard drive support	36h	ECC POST test single bit
1Eh	Reserved	37h-3Fh	Power-on password
1Fh	Power management functions	40-FFh	Feature Control/Status

NOTES:

Assume unmarked gaps are reserved.

Higher locations (>3Fh) contain information that should be accessed using the INT15, AX=E845h BIOS function (refer to Chapter 8 for BIOS function descriptions).

4.5 System Management

This section describes functions having to do with security, power management, temperature, and overall status. These functions are handled by hardware and firmware (BIOS) and generally configured through the Setup utility.

4.5.1 Security Functions

These systems include various features that provide different levels of security. Note that this subsection describes only the hardware functionality (including that supported by Setup) and does not describe security features that may be provided by the operating system and application software.

Power-On / Setup Password

These systems include a power-on and setup passwords, which may be enabled or disabled (cleared) through a jumper on the system board. The jumper controls a GPIO input to the 82801 ICH10 that is checked during POST. The password is stored in configuration memory (CMOS) and if enabled and then forgotten by the user will require that either the password be cleared (preferable solution and described below) or the entire CMOS be cleared (refer to section 4.4.1).

To clear the password, use the following procedure:

1. Turn off the system and disconnect the AC power cord from the outlet and/or system unit.
2. Remove the cover (hood) as described in the appropriate User Guide or Maintainance And Service Reference Guide. Insure that all system board LEDs are off (not illuminated).
3. Locate the password clear jumper (header is colored green and labeled E49 on these systems) and move the jumper from pins 1 and 2 and place on (just) pin 2 (for safekeeping).
4. Replace the cover.
5. Re-connect the AC power cord to the AC outlet and/or system unit.
6. Turn on the system. The POST routine will clear and disable the password.
7. To re-enable the password feature, repeat steps 1-6, replacing the jumper on pins 1 and 2 of header E49.

Setup Password

The Setup utility may be configured to be always changeable or changeable only by entering a password. Refer to the previous procedure (Power On / Setup Password) for clearing the Setup password.

Cable Lock Provision

These systems include a chassis cutout (on the rear panel) for the attachment of a cable lock mechanism.

I/O Interface Security

The SATA, serial, parallel, USB, and diskette interfaces may be disabled individually through the Setup utility to guard against unauthorized access to a system. In addition, the ability to write to or boot from a removable media drive (such as the diskette drive) may be enabled through the Setup utility. The disabling of the serial, parallel, and diskette interfaces are a function of the SIO controller. The USB ports are controlled through the 82801.

Chassis Security

Some systems feature Smart Cover (hood) Sensor and Smart Cover (hood) Lock mechanisms to inhibit unauthorized tampering of the system unit.

Smart Cover Sensor

These systems include a plunger switch that, when the cover (hood) is removed, closes and grounds an input of the 82801 component. The battery-backed logic will record this “intrusion” event by setting a specific bit. This bit will remain set (even if the cover is replaced) until the system is powered up and the user completes the boot sequence successfully, at which time the bit will be cleared. Through Setup, the user can set this function to be used by Alert-On-LAN and or one of three levels of support for a “cover removed” condition:

Level 0—Cover removal indication is essentially disabled at this level. During POST, status bit is cleared and no other action is taken by BIOS.

Level 1—During POST the message "The computer's cover has been removed since the last system start up" is displayed and time stamp in CMOS is updated.

Level 2—During POST the "The computer's cover has been removed since the last system start up" message is displayed, time stamp in CMOS is updated, and the user is prompted for the administrator password. (A Setup password must be enabled in order to see this option).

Smart Cover Lock (Optional)

The SFF and CMT systems support an optional solenoid-operated locking bar that, when activated, prevents the cover (hood) from being removed. The GPIO ports 44 and 45 of the SIO controller provide the lock and unlock signals to the solenoid. A locked hood may be bypassed by removing special screws that hold the locking mechanism in place. The special screws are removed with the Smart Cover Lock Failsafe Key.

4.5.2 Power Management

These systems provide baseline hardware support of ACPI- and APM-compliant firmware and software. Key power-consuming components (processor, chipset, I/O controller, and fan) can be placed into a reduced power mode either automatically or by user control. The system can then be brought back up ("wake-up") by events defined by the ACPI 2.0 specification. The ACPI wake-up events supported by this system are listed as follows:

Table 4-7.
ACPI Wake-Up Events

ACPI Wake-Up Event	System Wakes From
Power Button	Suspend or soft-off
RTC Alarm	Suspend or soft-off
Wake On LAN (w/NIC)	Suspend or soft-off
PME	Suspend or soft-off
Serial Port Ring	Suspend or soft-off
USB	Suspend only
Keyboard	Suspend only
Mouse	Suspend only

4.5.3 System Status

These systems provide a visual indication of system boot, ROM flash, and operational status through the power LED and internal speaker, as described in Table 4-8.

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Table 4-8.
System Operational Status LED Indications

System Status	PowerLED	Beeps [2]	Action Required
S0: System on (normal operation)	Steady green	None	None
S1: Suspend	Blinks green @ .5 Hz	None	None
S3: Suspend to RAM	Blinks green @ .5 Hz	None	None
S4: Suspend to disk	Off – clear	None	None
S5: Soft off	Off – clear	None	None
Processor thermal shutdown	Blinks red 2 times @ 1 Hz [1]	2	Check air flow, fans, heatsink
Processor not seated / installed	Blinks red 3 times @ 1 Hz [1]	3	Check processor presence/seating
Power supply overload failure	Blinks red 4 times @ 1 Hz [1]	4	Check system board problem [3],
Memory error (pre-video)	Blinks red 5 times @ 1 Hz [1]	5	Check DIMMs, system board
Video error	Blinks red 6 times @ 1 Hz [1]	6	Check graphics card or system board
PCA failure detected by BIOS (pre-video)	Blinks red 7 times @ 1 Hz [1]	7	Replace system board
Invalid ROM checksum error	Blinks red 8 times @ 1 Hz [1]	8	Reflash BIOS ROM
Boot failure (after power on)	Blinks red 9 times @ 1 Hz [1]	9	Check power supply, processor, sys. bd
Bad option card	Blinks red 10 times @ 1 Hz [1]	None	Replace option card

NOTES:

Beeps are repeated for 5 cycles, after which only blinking LED indication continues.

[1] Repeated after 2 second pause.

[2] Beeps are produced by the internal chassis speaker.

[3] Check that CPU power connector P3 is plugged in.

4.5.4 Thermal Sensing and Cooling

All systems feature a variable-speed fan mounted as part of the processor heatsink assembly. All systems also provide or support an auxiliary chassis fan. All fans are controlled through temperature sensing logic on the system board and/or in the power supply. There are some electrical differences between form factors and between some models, although the overall functionally is the same. Typical cooling conditions include the following:

1. Normal—Low fan speed.
2. Hot processor—ASIC directs Speed Control logic to increase speed of fan(s).
3. Hot power supply—Power supply increases speed of fan(s).
4. Sleep state—Fan(s) turned off. Hot processor or power supply will result in starting fan(s).

The RPM (speed) of all fans is the result of the temperature of the CPU as sensed by speed control circuitry. The fans are controlled to run at the slowest (quietest) speed that will maintain proper cooling.

Units using chassis and CPU fans must have both fans connected to their corresponding headers to ensure proper cooling of the system.

4.6 Register Map and Miscellaneous Functions

This section contains the system I/O map and information on general-purpose functions of the ICH10 and I/O controller.

4.6.1 System I/O Map

Table 4-9 lists the fixed addresses of the input/output (I/O) ports.

Table 4-9
System I/O Map

I/O Port	Function
0000..001Fh	DMA Controller 1
0020..002Dh	Interrupt Controller 1
002E, 002Fh	Index, Data Ports to SIO Controller (primary)
0030..003Dh	Interrupt Controller
0040..0042h	Timer 1
004E, 004Fh	Index, Data Ports to SIO Controller (secondary)
0050..0052h	Timer / Counter
0060..0067h	Microcontroller, NMI Controller (alternating addresses)
0070..0077h	RTC Controller
0080..0091h	DMA Controller
0092h	Port A, Fast A20/Reset Generator
0093..009Fh	DMA Controller
00A0..00B1h	Interrupt Controller 2
00B2h, 00B3h	APM Control/Status Ports
00B4..00BDh	Interrupt Controller
00C0..00DFh	DMA Controller 2
00F0h	Coprocessor error register
0170..0177h	IDE Controller 2 (active only if standard I/O space is enabled for secondary controller)
01F0..01F7h	IDE Controller 1 (active only if standard I/O space is enabled for primary controller)
0278..027Fh	Parallel Port (LPT2)
02E8..02EFh	Serial Port (COM4)
02F8..02FFh	Serial Port (COM2)
0370..0377h	Diskette Drive Controller Secondary Address
0376h	IDE Controller 2 (active only if standard I/O space is enabled for primary drive)
0378..037Fh	Parallel Port (LPT1)
03B0..03DFh	Graphics Controller
03BC..03BEh	Parallel Port (LPT3)
03E8..03EFh	Serial Port (COM3)
03F0..03F5h	Diskette Drive Controller Primary Addresses
03F6h	IDE Controller 1 (active only if standard I/O space is enabled for sec. drive)
03F8..03FFh	Serial Port (COM1)
04D0, 04D1h	Interrupt Controller
0678..067Fh	Parallel Port (LPT2)
0778..077Fh	Parallel Port (LPT1)
07BC..07BEh	Parallel Port (LPT3)
0CF8h	PCI Configuration Address (dword access only)
0CF9h	Reset Control Register
0CFCh	PCI Configuration Data (byte, word, or dword access)

NOTE:

Assume unmarked gaps are unused, reserved, or used by functions that employ variable I/O address mapping. Some ranges may include reserved addresses.

4.6.2 GPIO Functions

ICH10 Functions

The ICH10 provides various functions through the use of programmable general purpose input/output (GPIO) ports. These systems use GPIO ports and associate registers of the ICH10 for the following functions:

- PCI interupt request control
- Chassis and board ID
- Hood (cover) sensor and lock detect
- Media card reader detect
- S4 state indicator
- USB port over-current detect
- Flash security override
- Serial port detect
- REQn#/GNTn# sigal control
- Password enable
- Boot block enable

SIO Controller Functions

In addition to the serial and parallel port functions, the SIO controller provides the following specialized functions through GPIO ports:

- Power/Hard drive LED control for indicating system events (refer to Table 4-8)
- Hood lock/unlock controls the lock bar mechanism
- Thermal shutdown control turns off the CPU when temperature reaches certain level
- Processor present/speed detection detects if the processor has been removed. The occurrence of this event will, during the next boot sequence, initiate the speed selection routine for the processor.
- Legacy/ACPI power button mode control uses the pulse signal from the system's power button and produces the PS On signal according to the mode (legacy or ACPI) selected. Refer to chapter 7 for more information regarding power management.