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You can read the recommendations in the user guide, the technical guide or the installation guide for TRANSCEND TS1GCF200I. You'll find the answers to all your questions on the TRANSCEND TS1GCF200I in the user manual (information, specifications, safety advice, size, accessories, etc.). Detailed instructions for use are in the User's Guide.

User manual TRANSCEND TS1GCF200I  
User guide TRANSCEND TS1GCF200I  
Operating instructions TRANSCEND TS1GCF200I  
Instructions for use TRANSCEND TS1GCF200I  
Instruction manual TRANSCEND TS1GCF200I

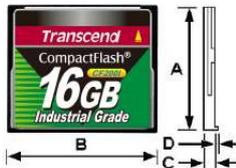
## Transcend Industrial CF Card TS128M~16GCF200I



### Description

The Transcend CF200I is a High Speed industrial Compact Flash Card with high quality Flash Memory assembled on a printed circuit board.

### Placement



### Dimensions

| Size | Millimeters   | Inches       |
|------|---------------|--------------|
| A    | 36.40 ± 0.150 | 1.43 ± 0.005 |
| B    | 42.80 ± 0.100 | 1.69 ± 0.004 |
| C    | 3.30 ± 0.100  | 0.13 ± 0.004 |
| D    | 0.63 ± 0.070  | 0.02 ± 0.003 |

### Features

- CompactFlash Specification Version 4.1 Compliant
- RoHS compliant products
- Single Power Supply: 3.3V±5% or 5V±10%
- Operating Temperature: -40°C to 85°C
- Storage Temperature: -55°C to 100°C
- Humidity (No n condensation): 0% to 95%
- Built-in 13/24-bit ECC (Error Correction Code) functionality and wear-leveling algorithm ensures highly reliable of data transfer
- ✓ 13bit BCH ECC (2k+64 / 4k+128 byte per page flash)
- ✓ 24bit BCH ECC (4k+208 byte per page flash)
- Operation Modes:
  - ✓ PC Card Memory Mode
  - ✓ PC Card IO Mode
  - ✓ True DE Mode
- True IDE Mode supports:
  - ✓ Ultra DMA Mode 0 to 5 (UDMA4 as default)
  - ✓ Multi-Word DMA Mode 0 to 4
  - ✓ PIO Mode 0 to 6
- True IDE Mode: Fixed Disk (Default)
- PC Card Mode: Fixed Disk (Default)
- Durability of Connector: 10,000 times
- MTBF: 4,000,000 hours (in 25°C)
- Support Global Wear-Leveling, Static Data Refresh, Early Retirement, and Erase Count Monitor functions to extend product life
- Support S.M.A.R.T (Self-defined)
- Support Security Command
- Compliant to CompactFlash, PCMCIA, and ATA standards



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**Manual abstract:**

StandBy Current : 5V : 2.8mA 3.3V : 2.2mA 3. @@@@ (2) Find the static-block and save it in wear-leveling pointer. (3) Check the erase count when the block popped from spare pool. If the block erase count is bigger than WEARCNT, then swapped the static-block and over-count-block. After actual test, global wear leveling successfully even the erase count of every block; hence, it can extend the life expectancy of Flash product. 2. StaticDataRefresh Technology Keeping Data Healthy There are many variants that would disturb the charge inside a Flash cell. These variants can be: time, read operations, undesired charge, heat, etc; each variant would create a charge loss, and the contents shift in their charge levels slightly. @@@@ @@@@ This implementation practically restores the data to its original, error-free state, and hence, lengthening the life of the data. 3. EarlyRetirement Avoiding Data Loss Due to Weak Block The StaticDataRefresh feature functions well when the cells in a block are still healthy. As the block ages over time, it cannot store charge reliably anymore, EarlyRetirement enters the scene. EarlyRetirement works by moving the static data to another block (a health block) before the previously used block becomes completely incapable of holding charges for data. When the charge loss error level exceeds another threshold value (higher from that for StaticDataRefresh), the controller automatically moves its data to another block. In addition, the original block is then marked as a bad block, which prevents its further use, and thus the block enters the state of "EarlyRetirement." Note that, through this process, the incorrect data are detected and effectively corrected by the ECC engine, thus the data in the new block is stored error-free. Transcend Information Inc.

4 V1.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Transcend Transcend Information Inc. 5 V1.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Block Diagram Transcend Information Inc. 6 V1.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Pin Assignments and Pin Type Transcend Information Inc. 7 V1.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Note: 1) These signals are required only for 16 bit accesses and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current. 2) The signal should be grounded by the host.

3) The signal should be tied to VCC by the host. 4) The mode is required for CompactFlash Storage Cards. 5) The -CSEL signal is ignored by the card in PC Card modes. However, because it is not pulled upon the card in these modes, it should not be left floating by the host in PC Card modes. In these modes, the pin should be connected by the host to PC Card A25 or grounded by the host. 6) If DMA operations are not used, the signal should be held high or tied to VCC by the host. For proper operation in older hosts: while DMA operations are not active, the card shall ignore this signal, including a floating condition 7) Signal usage in True IDE Mode except when Ultra DMA mode protocol is active. 8) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Write is active. 9) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Read is active. 10) Signal usage in PC Card I/O and Memory Mode when Ultra DMA mode protocol DMA Write is active. 11) Signal usage in PC Card I/O and Memory Mode when Ultra DMA mode protocol DMA Read is active. 12) Signal usage in PC Card I/O and Memory Mode when Ultra DMA protocol is active. Transcend Information Inc. 8 V1.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Signal Description Signal Name A10 A00 (PC Card Memory Mode) Dir. I Pin Description 8,10,11,12, These address lines along with the -REG signal are used to select the following: 14,15,16,17, The I/O port address registers within the CompactFlash Storage Card, the memory mapped port address registers within the CompactFlash Storage Card, 18,19,20 a byte in the card's information structure and its configuration control and status registers. This signal is the same as the PC Card Memory Mode signal. A10 A00 (PC Card I/O Mode) A02 - A00 (True IDE Mode) I 18,19,20 In True IDE Mode, only A[02:00] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host. This signal is asserted high, as BVD1 is not supported. BVD1 (PC Card Memory Mode) -STSCHG (PC Card I/O Mode) Status Changed -PDIAG (True IDE Mode) BVD2 (PC Card Memory Mode) -SPKR (PC Card I/O Mode) -DASP (True IDE Mode) -CD1, -CD2 (PC Card Memory Mode) I/O 46 This signal is asserted low to alert the host to changes in the READY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register. In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol. I/O 45 This signal is asserted high, as BVD2 is not supported. This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated. In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol. O 26,25 These Card Detect pins are connected to ground on the CompactFlash Storage Card. They are used by the host to determine that the CompactFlash Storage Card is fully inserted into its socket. This signal is the same for all modes. -CD1, -CD2 (PC Card I/O Mode) -CD1, -CD2 (True IDE Mode) This signal is the same for all modes.

Transcend Information Inc. 9 V1.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Signal Name -CE1, -CE2 (PC Card Memory Mode) Card Enable Dir. I Pin 7,32 Description These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7. See Table 27, Table 29, Table 31, Table 35, Table 36 and Table 37. This signal is the same as the PC Card Memory Mode signal. -CE1, -CE2 (PC Card I/O Mode) Card Enable -CS0, -CS1 (True IDE Mode) In the True IDE Mode, -CS0 is the address range select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register. While DMACK is asserted, -CS0 and CS1 shall be held negated and the width of the transfers shall be 16 bits. -CSEL (PC Card Memory Mode) -CSEL (PC Card I/O Mode) -CSEL (True IDE Mode) I 39 This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.



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This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host. This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave. D15 - D00 (PC Card Memory Mode) I/O 31,30,29,28, These lines carry the Data, Commands and Status information between the host 27,49,48,47, and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB 6,5,4,3,2, of the Odd Byte of the Word. 23, 22, 21 This signal is the same as the PC Card Memory Mode signal.

DMODE. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol. In True IDE Mode, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst. STOP (True IDE Mode Ultra DMA Protocol Active) -OE (PC Card Memory Mode) I 9 This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Storage Card in Memory Mode and to read the CIS and configuration registers. In PC Card I/O Mode, this signal is used to read the CIS and configuration registers. To enable True IDE Mode this input should be grounded by the host. -OE (PC Card I/O Mode) -ATA SEL (True IDE Mode) READY (PC Card Memory Mode) O 37 In Memory Mode, this signal is set high when the CompactFlash Storage Card is ready to accept a new data transfer operation and is held low when the card is busy. At power up and at Reset, the READY signal is held low (busy) until the CompactFlash Storage Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card during this time.

Note, however, that when a card is powered up and used with RESET continuously disconnected or asserted, the Reset function of the RESET pin is disabled. Consequently, the continuous assertion of RESET from the application of power shall not cause the READY signal to remain continuously in the busy state.

-IRQ (PC Card I/O Mode) I/O Operation After the CompactFlash Storage Card has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt. In True IDE Mode signal is the active high Interrupt Request to the host. INTRQ (True IDE Mode) Transcend Information Inc. 12 V1.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Signal Name -REG (PC Card Memory Mode) Attribute Memory Select -REG (PC Card I/O Mode) -DMACK (True IDE Mode) Dir. I Pin 44 Description This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.

The signal shall also be active (low) during I/O Cycles when the I/O address is on the Bus. This is a DMA Acknowledge signal that is asserted by the host in response to DMARQ to initiate DMA transfers. While DMA operations are not active, the card shall ignore the -DMACK signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation all modes.

RESET (PC Card Memory Mode) I 41 The CompactFlash Storage Card is Reset when the RESET pin is high with the following important exception: The host may leave the RESET pin open or keep it continually high from the application of power without causing a continuous Reset of the card. Under either of these conditions, the card shall emerge from power-up having completed an initial Reset. The CompactFlash Storage Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set. RESET (PC Card I/O Mode) -RESET (True IDE Mode) VCC (PC Card Memory Mode) VCC (PC Card I/O Mode) VCC (True IDE Mode) This signal is the same as the PC Card Memory Mode signal. In the True IDE Mode, this input pin is the active low hardware reset from the host.

-- 13,38 +5 V, +3.3 V power. This signal is the same for all modes. This signal is the same for all modes. Transcend Information Inc. 13 V1.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Signal Name -VS1 -VS2 (PC Card Memory Mode) -VS1 -VS2 (PC Card I/O Mode) -VS1 -VS2 (True IDE Mode) -WAIT (PC Card Memory Mode) -WAIT (PC Card I/O Mode) IORDY (True IDE Mode Except Ultra DMA Mode) -DDMARDY (True IDE Mode Ultra DMA Write Mode) Dir. O Pin 33 40 Description Voltage Sense Signals. -VS1 is grounded on the Card and sensed by .8 40 40 2.

0 0.8 1.2 Min. 2.7 2.4 0.4 Max. 3.6 Unit V V V V V V V kOhm kOhm Non-schmitt trigger Schmitt trigger Non-schmitt trigger Schmitt trigger Remark 1. Include CE1, CE2, HREG, HOE.

HIOE, HWE, HIOV pins. 2. Include CE1, CE2, HREG, HOE. HIOE, HWE, HIOV, CSEL, PDIAG, DASP pins. Transcend Information Inc. 16 V1.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Output Drive Type Output Drive Characteristics Transcend Information Inc. 17 V1.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Signal Interface Transcend Information Inc. 18 VI.

2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Notes: 1) Control Signals: each card shall present a load to the socket no larger than 50 pF 10 at a DC current of 700 A low state and 150 A high state, including pull-resistor. The socket shall be able to drive at least the following load 10 while meeting all AC timing requirements: (the number of sockets wired in parallel) multiplied by (50 pF with DC current 700 A low state and 150 A high state per socket). 2) Resistor is optional. 3) Status Signals: the socket shall present a load to the card no larger than 50 pF 10 at a DC current of 400 A low 10 while meeting all AC timing requirements: 50 pF at a DC current of 400 A low state and 1100 A high state. 6) BVD2 was not defined in the JEIDA 3.0 release. Systems fully supporting JEIDA release 3 SRAM cards shall pull-up pin 45 (BVD2) to avoid sensing their batteries as "Low." 7) Address Signals: each card shall present a load of no more than 100pF 10 at a DC current of 450 A low state and 150 A high state. The host shall be able to drive at least the following load 10 while meeting all AC timing requirements: (the number of sockets wired in parallel) multiplied by (100pF with DC current 450 A low state and 150 A high state per socket).



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8) Data Signals: the host and each card shall present a load no larger than 50pF 10 at a DC current of 450 A and 150 A high state.

The host and each card shall be able to drive at least the following load 10 while meeting all AC timing requirements: 100pF with DC current 1.6mA low state and 300 A high state. This permits the host to wire two sockets in parallel without derating the card access speeds. 9) Reset Signal: This signal is pulled up to prevent the input from floating when a CFA to PCMCIA adapter is used in a PCMCIA revision 1 host. However, to minimize DC current drain through the pull-up resistor in normal operation the pull-up should be turned off once the Reset signal has been actively driven low by the host. Consequently, the input is specified as an I2Z because the resistor is not necessarily detectable in the input current leakage test. 10) Host and card restrictions for CF Advanced Timing Modes and Ultra DMA modes: Additional Requirements for CF Advanced Timing Modes and Ultra DMA Electrical Requirements for additional required limitations on the implementation of CF Advanced Timing modes and Ultra DMA modes respectively. Additional Requirements for CF Advanced Timing Modes The CF Advanced Timing modes include PCMCIA I/O and Memory modes that are 100ns or faster and True IDE PIO Modes 5,6 and Multiword DMA Modes 3,4. When operating in CF Advanced timing modes, the host shall conform to the following requirements: 1) Only one CF device shall be attached to the CF Bus. 2) The host shall not present a load of more than 40pF to the device for all signals, including any cabling. 3) The maximum cable length is 0.15 m (6 in). The cable length is measured from the card connector to the host controller. 0.46 m (18 in) cables are not supported.

4) The -WAIT and IORDY signals shall be ignored by the host. Devices supporting CF Advanced timing modes shall also support slower timing modes, to ensure operability with systems that do not support CF Advanced timing modes Transcend Information Inc. 19 V1.2 state and 100 A high state, including pull-up resistor. The card shall be able to drive at least the following load 5) Status Signals: the socket shall present a load to the card no larger than 50 pF 10 at a DC current of 400 10 while meeting all AC timing requirements: 50 pF at a DC current of 400 state and 100 A high state, including pull-up resistor. The card shall be able to drive at least the following load A low state and 100 A high state. A low 4) Status Signals: the socket shall present a load to the card no larger than 50 pF 10 at a DC current of 400 10 while meeting all AC timing requirements: 50 pF at a DC current of 400 state and 100 A high state, including pull-up resistor. The card shall be able to drive at least the following load A low state and 100 A high state. A low Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Ultra DMA Electrical Requirements Host and Card signal capacitance limits for Ultra DMA operation The host interface signal capacitance at the host connector shall be a maximum of 25 pF for each signal as measured at 1 MHz. The card interface signal capacitance at the card connector shall be a maximum of 20 pF for each signal as measured at 1 MHz. Series termination required for Ultra DMA operation Series termination resistors are required at both the host and the card for operation in any of the Ultra DMA modes. Table 13 describes typical values for series termination at the host and the device. Signal Table: Typical Series Termination for Ultra DMA Transcend Information Inc. 20 V1.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Table: Ultra DMA Termination with Pull-up or Pull down Example Printed Circuit Board (PCB) Trace Requirements for Ultra DMA On any PCB for a host or device supporting Ultra DMA: The longest D[15:00] trace shall be no more than 0.

5" longer than either STROBE trace as measured from the IC pin to the connector. The shortest D[15:00] trace shall be no more than 0.5" shorter than either STROBE trace as measured from the IC pin to the connector. Ultra DMA Mode Cabling Requirement Operation in Ultra DMA mode requires a crosstalk suppressing cable. The cable shall have a grounded line between each signal line. For True IDE mode operation using a cable with IDE (ATA) type 40 pin connectors it is recommended that the host sense the cable type using the method described in the ANSI INCITS 361-2002 AT Attachment - 6 standard, to prevent use of Ultra DMA with a 40 conductor cable. Transcend Information Inc. 21 V1.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Attribute Memory Read Timing Specification Transcend Information Inc. 22 V1.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Configuration Register (Attribute Memory) Write Timing Specification Transcend Information Inc. 23 V1.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Common Memory Read Timing Specification Transcend Information Inc. 24 V1.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Common Memory Write Timing Specification Transcend Information Inc. 25 V1.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 I/O Input (Read) Timing Specification Transcend Information Inc. 26 V1.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 I/O Output (Write) Timing Specification Transcend Information Inc. 27 V1.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Transcend Information Inc. 28 V1.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 True IDE PIO Mode Read/Write Timing Specification Transcend Information Inc. 29 V1.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Transcend Information Inc. 30 V1.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Transcend Information Inc. 31 V1.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 True IDE Ultra DMA Mode Read/Write Timing Specification Table: Ultra DMA Data Burst Timing Transcend Information Inc. 32 V1.

2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Notes: 1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V. 2) All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of tRFS, both STROBE and DMARDY transitions are measured at the sender connector.



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3) The parameter tCYC shall be measured at the recipient's connector farthest from the sender. 4)The parameter tLI shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector. 5)The parameter tAZ shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus the allow for a bus turnaround. Transcend Information Inc. 33 VI.

2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Transcend Information Inc. 34 VI.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Notes: 1) The parameters tUI, tMLI : (Ultra DMA Data-In Burst Device Termination Timing and Ultra DMA Data-In Burst Host Termination Timing), and tLI indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding.

tUI is an unlimited interlock that has no maximum time value. tMLI is a limited time-out that has a defined minimum. tLI is a limited time-out that has a defined maximum. 2) 80-conductor cabling shall be required in order to meet setup (tDS, tCS) and hold (tDH, tCH) times in modes greater than 2. 3) Timing for tDVS, tDVH, tCVS and tCVH shall be met for lumped capacitive loads of 15 and 40 pF at the connector where the Data and STROBE signals have the same capacitive load value.

Due to reflections on the cable, these timing measurements are not valid in a normally functioning system. 4)For all modes the parameter tZIORDY may be greater than tENV due to the fact that the host has a pull-up on IORDY- giving it a known state when released. 5)The parameters tDS, and tDH for mode 5 are defined for a recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for tDS and tDH for mode 5 at the middle connector being 3.0 and 3.9 ns respectively. 6)The parameters are applied to True IDE mode operationonly.

Table: Ultra DMA Sender and Recipient IC Timing Requirements Notes: 1) All timing measurement switching points(low to high and high to low) shall be taken at 1.5 V. 2) The correct data value shall be captured by the recipient given input data with a slew rate of 0.

4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at tDSIC and tDHIC timing (as measured through 1.5 V). 3) The parameters tDVSIC and tDVHIC shall be met for lumped capacitive loads of 15 and 40 pF at the IC where all signals have the same capacitive load value.

Noise that may couple onto the output signals from external sources has not been included in these values. Transcend Information Inc. 35 VI.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Table: Ultra DMA Sender and Recipient IC Timing Requirements Note: 1) The sender shall be tested while driving an 18 inch long, 80 conductor cable with PVC insulation material. The signal under test shall be cut at a test point so that it has not trace, cable or recipient loading after the test point. All other signals should remain connected through to the recipient. The test point may be located at any point between the sender's series termination resistor and one half inch or less of conductor exiting the connector. If the test point is on a cable conductor rather than the PCB, an adjacent ground conductor shall also be cut within one half inch of the connector. The test load and test points should then be soldered directly to the exposed source side connectors. The test loads consist of a 15 pF or a 40 pF, 5%, 0.08 inch by 0.

05 inch surface mount or smaller size capacitor from the test point to ground. Slew rates shall be met for both capacitor values. Measurements shall be taken at the test point using a <1 pF, >100 Kohm, 1 Ghz or faster probe and a 500 MHz or faster oscilloscope. The average rate shall be measured from 20% to 80% of the settled VOH level with data transitions at least 120 nsec apart. The settled VOH level shall be measured as the average output high level under the defined testing conditions from 100 nsec after 80% of a rising edge until 20% of the subsequent falling edge.

Transcend Information Inc. 36 VI.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Card Configuration The CompactFlash Storage Cards is identified by appropriate information in the Card Information Structure (CIS). The following configuration registers are used to coordinate the I/O spaces and the Interrupt level of cards that are located in the system. In addition, these registers provide a method for accessing status information about the CompactFlash Storage Card that may be used to arbitrate between multiple interrupt sources on the same interrupt level or to replace status information that appears on dedicated pins in memory cards that have alternate use in I/O cards. Multiple Function CompactFlash Storage Cards Table: CompactFlash Storage Card Registers and Memory Space Decoding Table: CompactFlash Storage Card Configuration Registers Decoding Transcend Information Inc. 37 VI.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Attribute Memory Function Attribute memory is a space where CompactFlash Storage Card identification and configuration information are stored, and is limited to 8 bit wide accesses only at even addresses. The card configuration registers are also located here. For CompactFlash Storage Cards, the base address of the ard configuration registers is 200h.

Table 31: Attribute Memory Function Transcend Information Inc. 38 VI.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Configuration Option Register (Base + 00h in Attribute Memory) Transcend Information Inc. 39 VI.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Card Configuration and Status Register (Base + 02h in Attribute Memory) Transcend Information Inc. 40 VI.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Pin Replacement Register (Base + 04h in Attribute Memory) Transcend Information Inc. 41 VI.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Socket and Copy Register (Base + 06h in Attribute Memory) Transcend Information Inc. 42 VI.

2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 I/O Transfer Function The I/O transfer to or from the CompactFlash Storage can be either 8 or 16 bits. When a 16 bit accessible port is addressed, the signal -IOIS16 is asserted by the CompactFlash Storage.



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Otherwise, the -IOIS16 signal is de-asserted. When a 16 bit transfer is attempted, and the -IOIS16 signal is not asserted by the CompactFlash Storage, the system shall generate a pair of 8 bit references to access the word's even byte and odd byte. The CompactFlash Storage Card permits both 8 and 16 bit accesses to all of its I/O addresses, so -IOIS16 is asserted for all addresses to which the CompactFlash Storage responds.

The CompactFlash Storage Card may request the host to extend the length of an input cycle until data is ready by asserting the -WAIT signal at the start of the cycle. Table : PCMCIA Mode I/O Function Transcend Information Inc. 43 VI.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Common Memory Transfer Function The Common Memory transfer to or from the CompactFlash Storage can be either 8 or 16 bits. Table: Common Memory Function Transcend Information Inc.

44 VI.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 True IDE Mode I/O Transfer Function The CompactFlash Storage Card can be configured in a True IDE Mode of operation. The CompactFlash Storage Card is configured in this mode only when the -OE input signal is grounded by the host during the power off to power on cycle. Optionally, CompactFlash Storage Cards may support the following optional detection methods: 1. The card is permitted to monitor the OE (-ATA SEL) signal at any time(s) and switch to PCMCIA mode upon detecting a high level on the pin. 2. The card is permitted to re-arbitrate the interface mode determination following a transition of the (-)RESET pin. 3. The card is permitted to monitor the OE (-ATA SEL) signal at any time(s) and switch to True IDE mode upon detection of a continuous low level on pin for an extended period of time. Table: True IDE Mode I/O Function defines the function of the operations for the True IDE Mode.

Transcend Information Inc. 45 VI.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Metaformat Overview The goal of the Metaformat is to describe the requirements and capabilities of the CompactFlash Storage Card as thoroughly as possible. This includes describing the power requirements, IO requirements, memory requirements, manufacturer information and details about the services provided.

Table: Sample Device Info Tuple Information for Extended Speeds Note: The value "1" defined for D3 of the N+0 words indicates that no write-protect switch controls writing the ATA registers. The value "0" defined for D7 in the N+2 words indicates that there is not more than a single speed extension byte.

Transcend Information Inc. 46 VI.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 CF-ATA Drive Register Set Definition and Protocol The CompactFlash Storage Card can be configured as a high performance I/O device through: a) The standard PC-AT disk I/O address spaces 1F0h-1F7h, 3F6h-3F7h (primary) or 170h- 177h, 376h-377h (secondary) with IRQ 14 (or other available IRQ). b) Any system decoded 16 byte I/O block using any available IRQ.

c) Memory space. The communication to or from the CompactFlash Storage Card is done using the Task File registers, which provide all the necessary registers for control and status information related to the storage medium. The PCMCIA interface connects peripherals to the host using four register mapping methods. Table 39 is a detailed description of these methods: Transcend Information Inc. 47 VI.

2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 I/O Primary and Secondary Address Configurations Table: Primary and Secondary I/O Decoding Transcend Information Inc. 48 VI.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Contiguous I/O Mapped Addressing When the system decodes a contiguous block of I/O registers to select the CompactFlash Storage Card, the registers are accessed in the block of I/O space decoded by the system as follows: Table: Contiguous I/O Decoding Transcend Information Inc. 49 VI.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Memory

Mapped Addressing When the CompactFlash Storage Card registers are accessed via memory references, the registers appear in the common memory space window: 0-2K bytes as follows: True IDE Mode Addressing When the CompactFlash Storage Card is configured in the True IDE Mode, the I/O decoding is as follows: Transcend Information Inc.

50 VI.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 CF-ATA Registers The following section describes the hardware registers used by the host software to issue commands to the CompactFlash device. These registers are often collectively referred to as the "task file." Data Register (Address - 1F0h[170h]; Offset 0,8,9) The Data Register is a 16 bit register, and it is used to transfer data blocks between the CompactFlash Storage Card data buffer and the Host. This register overlaps the Error Register. Error Register (Address - 1F1h[171h]; Offset 1, 0Dh Read Only) This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. This register is also accessed in PC Card Modes on data bits D15-D8 during a read operation to offset 0 with -CE2 low and -CE1 high. Bit 7 (BBK/ICRC): this bit is set when a Bad Block is detected. This bit is also set when an interface CRC error is detected in True IDE Ultra DMA modes of operation. Bit 6 (UNC): this bit is set when an Uncorrectable Error is encountered.

Bit 5: this bit is 0. Bit 4 (IDNF): the requested sector ID is in error or cannot be found. Bit 3: this bit is 0. Bit 2 (Abort) This bit is set if the command has been aborted because of a CompactFlash Storage Card status condition: (Not Ready, Write Fault, etc.) or when an invalid command has been issued. Bit 1 This bit is 0. Bit 0 (AMNF) This bit is set in case of a general error. Transcend Information Inc. 51 VI.2 Transcend Industriall CF Card Transcend ndustr a CF Card TS128M~16GCF200II TS128M~16GCF200 Feature Register (Address - 1F1h[171h]; Offset 1, 0Dh Write Only) This register provides information regarding features of the CompactFlash Storage Card that the host can utilize.

This register is also accessed in PC Card modes on data bits D15-D8 during a write operation to Offset 0 with -CE2 low and -CE1 high. Sector Count Register (Address - 1F2h[172h]; Offset 2) This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the CompactFlash Storage Card. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion.



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*Bit 11: IORDY Supported* If bit 11 is set to 1 then this CompactFlash Storage Card supports IORDY operation. If bit 11 is set to 0 then this CompactFlash Storage Card may support IORDY operation. *Bit 10: IORDY may be disabled* Bit 10 shall be set to 0, indicating that IORDY may not be disabled. *Bit 9: LBA supported* Bit 9 shall be set to 1, indicating that this CompactFlash Storage Card supports LBA mode addressing.

*CF devices shall support LBA addressing.* *Bit 8: DMA Supported* If bit 8 is set to 1 then Read DMA and Write DMA commands are supported. Bit 8 shall be set to 0. *Read/Write DMA commands are not currently permitted on CF cards.* *PIO Data Transfer Cycle Timing Mode* The PIO transfer timing for each CompactFlash Storage Card falls into modes that have unique parametric timing specifications.

*The value returned in Bits 15-8 shall be 00h for mode 0, 01h for mode 1, or 02h for mode 2. Values 03h through FFh are reserved.* *Translation Parameters Valid* Bit 0 shall be set to 1 indicating that words 54 to 58 are valid and reflect the current number of cylinders, heads and sectors. If bit 1 of word 53 is set to 1, the values in words 64 through 70 are valid. If this bit is cleared to 0, the values reported in words 64-70 are not valid.

*Any CompactFlash Storage Card that supports PIO mode 3 or above shall set bit 1 of word 53 to one and support the fields contained in words 64 through 70.* *Current Number of Cylinders, Heads, Sectors/Track* These fields contains the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode. *Current Capacity* This field contains the product of the current cylinders times heads times sectors. *Multiple Sector Setting* Bits 15-9 are reserved and shall be set to 0. Bit 8 shall be set to 1 indicating that the Multiple Sector Setting is valid. Bits 7-0 are the current setting for the number of sectors that shall be transferred per interrupt on Read/Write Multiple commands. *Total Sectors Addressable in LBA Mode* This field contains the total number of user addressable sectors for the CompactFlash Storage Card in LBA mode only. *Multiword DMA transfer* Bits 15 through 8 of word 63 of the Identify Device parameter information is defined as the Multiword DMA mode selected field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant.

*Only one of bits may be set to one in this field by the CompactFlash Storage Card to indicate the multiword DMA mode which is currently selected.* Of these bits, bits 15 through 11 are reserved. Bit 8, if set to one, Transcend Information Inc. 78 V1.2 Transcend Industriall CF Card Transcend industr a CF Card TS128M~16GCF200II TS128M~16GCF200 indicates that Multiword DMA mode 0 has been selected. Bit 9, if set to one, indicates that Multiword DMA mode 1 has been selected. Bit 10, if set to one, indicates that Multiword DMA mode 2 has been selected. Selection of Multiword DMA modes 3 and above are specific to CompactFlash are reported in word 163, Word 163: CF Advanced True IDE Timing Mode Capabilities and Settings. Bits 7 through 0 of word 63 of the Identify Device parameter information is defined as the Multiword DMA data transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one.

*This field is bit significant.* Any number of bits may be set to one in this field by the CompactFlash Storage Card to indicate the Multiword DMA modes it is capable of supporting. Of these bits, bits 7 through 2 are reserved. Bit 0, if set to one, indicates that the CompactFlash Storage Card supports Multiword DMA mode 0. Bit 1, if set to one, indicates that the CompactFlash Storage Card supports Multiword DMA modes 1 and 0.

Bit 2, if set to one, indicates that the CompactFlash Storage Card supports Multiword DMA modes 2, 1 and 0. Support for Multiword DMA modes 3 and above are specific to CompactFlash are reported in word 163, Word 163: CF Advanced True IDE Timing Mode Capabilities and Settings. Word 64: Advanced PIO transfer modes supported Bits 7 through 0 of word 64 of the Identify Device parameter information is defined as the advanced PIO data transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant.

Any number of bits may be set to one in this field by the CompactFlash Storage Card to indicate the advanced PIO modes it is capable of supporting. Of these bits, bits 7 through 2 are reserved. Bit 0, if set to one, indicates that the CompactFlash Storage Card supports PIO mode 3. Bit 1, if set to one, indicates that the CompactFlash StorageCard supports PIO mode 4. Support for PIO modes 5 and above are specific to CompactFlash are reported in word 163, Word 65: Minimum Multiword DMA transfer cycle time Word 65 of the parameter information of the Identify Device command is defined as the minimum Multiword DMA transfer cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the CompactFlash Storage Card guarantees data integrity during the transfer. If this field is supported, bit 1 of word 53 shall be set to one. The value in word 65 shall not be less than the minimum cycle time for the fastest DMA mode supported by the device. This field shall be supported by all CompactFlash Storage Cards supporting DMA modes 1 and above.

If bit 1 of word 53 is set to one, but this field is not supported, the Card shall return a value of zero in this field. *Recommended Multiword DMA transfer cycle time* Word 66 of the parameter information of the Identify Device command is defined as the recommended Multiword DMA transfer cycle time. This field defines, in nanoseconds, the cycle time that, if used by the host, may optimize the data transfer from by reducing the probability that the CompactFlash Storage Card will need to negate the DMARQ signal during the transfer of a sector. If this field is supported, bit 1 of word 53 shall be set to one. The value in word 66 shall not be less than the value in word 65. This field shall be supported by all CompactFlash Storage Cards supporting DMA modes 1 and above. If bit 1 of word 53 is set to one, but this field is not supported, the Card shall return a value of zero in this field. *Word 67: Minimum PIO transfer cycle time without flow control* Word 67 of the parameter information of the Identify Device command is defined as the minimum PIO transfer without flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the CompactFlash Storage Card guarantees data integrity during the transfer without utilization of flow control. If this field is supported, Bit 1 of word 53 shall be set to one.

Any CompactFlash Storage Card that supports PIO mode 3 or above shall support this field, and the value in word 67 shall not be less than the value reported in word 68. If bit 1 of word 53 is set to one because a CompactFlash Storage Card supports a field in words 64-70 other than this field and the CompactFlash Storage Card does not support this field, the CompactFlash Storage Card shall return a value of zero in this field.



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Transcend Information Inc. 79 V1.2 Transcend Industrial CF Card Transcend Industrial CF Card TS128M~16GCF200II TS128M~16GCF200 Word 68: Minimum PIO transfer cycle time with IORDY Word 68 of the parameter information of the Identify Device command is defined as the minimum PIO transfer with IORDY flow control cycle time.

This field defines, in nanoseconds, the minimum cycle time that the CompactFlash Storage Card supports while performing data transfers while utilizing IORDY flow control. If this field is supported, Bit 1 of word 53 shall be set to one. Any CompactFlash Storage Card that supports PIO mode 3 or above shall support this field, and the value in word 68 shall be the fastest defined PIO mode supported by the CompactFlash Storage Card. If bit 1 of word 53 is set to one because a CompactFlash Storage Card supports a field in words 64-70 other than this field and the CompactFlash Storage Card does not support this field, the CompactFlash Storage Card shall return a value of zero in this field. Words 82-84: Features/command sets supported Words 82, 83, and 84 shall indicate features/command sets supported.

The value 0000h or FFFFh was placed in each of these words by CompactFlash Storage Cards prior to ATA-3 and shall be interpreted by the host as meaning that features/command sets supported are not indicated. Bits 1 through 13 of word 83 and bits 0 through 13 of word 84 are reserved. Bit 14 of word 83 and word 84 shall be set to one and bit 15 of word 83 and word 84 shall be cleared to zero to provide indication that the features/command sets supported words are valid. The values in these words should not be depended on by host implementers. Bit 0 of word 82 shall be set to zero; the SMART feature set is not supported. If bit 1 of word 82 is set to one, the Security Mode feature set is supported. Bit 2 of word 82 shall be set to zero; the Removable Media feature set is not supported. Bit 3 of word 82 shall be set to one; the Power Management feature set is supported. Bit 4 of word 82 shall be set to zero; the Packet Command feature set is not supported. If bit 5 of word 82 is set to one, write cache is supported.

If bit 6 of word 82 is set to one, look-ahead is supported. Bit 7 of word 82 shall be set to zero; release interrupt is not supported. Bit 8 of word 82 shall be set to zero; Service interrupt is not supported. Bit 9 of word 82 shall be set to zero; the Device Reset command is not supported. Bit 10 of word 82 shall be set to zero; the Host Protected Area feature set is not supported. Bit 11 of word 82 is obsolete. Bit 12 of word 82 shall be set to one; the CompactFlash Storage Card supports the Write Buffer command. Bit 13 of word 82 shall be set to one; the CompactFlash Storage Card supports the Read Buffer command. Bit 14 of word 82 shall be set to one; the CompactFlash Storage Card supports the NOP command. Bit 15 of word 82 is obsolete.

Bit 0 of word 83 shall be set to zero; the CompactFlash Storage Card does not support the Download Microcode command. Bit 1 of word 83 shall be set to zero; the CompactFlash Storage Card does not support the Read DMA Queued and Write DMA Queued commands. Bit 2 of word 83 shall be set to one; the CompactFlash Storage Card supports the CFA feature set. If bit 3 of word 83 is set to one, the CompactFlash Storage Card supports the Advanced Power Management feature set. Bit 4 of word 83 shall be set to zero; the CompactFlash Storage Card does not support the Removable Media Status feature set. Words 85-87: Features/command sets enabled Words 85, 86, and 87 shall indicate features/command sets enabled. The value 0000h or FFFFh was placed in each of these words by CompactFlash Storage Cards prior to ATA-4 and shall be interpreted by the host as meaning that features/command sets enabled are not indicated. Bits 1 through 15 of word 86 are reserved. Bits 0-13 of word 87 are reserved. Bit 14 of word 87 shall be set to one and bit 15 of word 87 shall be cleared to zero to provide indication that the features/command sets enabled words are valid.

The values in these words should not be depended on by host implementers. Transcend Information Inc. 80 V1.2 Transcend Industrial CF Card Transcend Industrial CF Card TS128M~16GCF200II TS128M~16GCF200 Bit 0 of word 85 shall be set to zero; the SMART feature set is not enabled. If bit 1 of word 85 is set to one, the Security Mode feature set has been enabled via the Security Set Password command. Bit 2 of word 85 shall be set to zero; the Removable Media feature set is not supported. Bit 3 of word 85 shall be set to one; the Power Management feature set is supported. Bit 4 of word 85 shall be set to zero; the Packet Command feature set is not enabled. If bit 5 of word 85 is set to one, write cache is enabled. If bit 6 of word 85 is set to one, look-ahead is enabled.

Bit 7 of word 85 shall be set to zero; release interrupt is not enabled. Bit 8 of word 85 shall be set to zero; Service interrupt is not enabled. Bit 9 of word 85 shall be set to zero; the Device Reset command is not supported. Bit 10 of word 85 shall be set to zero; the Host Protected Area feature set is not supported. Bit 11 of word 85 is obsolete. Bit 12 of word 85 shall be set to one; the CompactFlash Storage Card supports the Write Buffer command. Bit 13 of word 85 shall be set to one; the CompactFlash Storage Card supports the Read Buffer command. Bit 14 of word 85 shall be set to one; the CompactFlash Storage Card supports the NOP command. Bit 15 of word 85 is obsolete. Bit 0 of word 86 shall be set to zero; the CompactFlash Storage Card does not support the Download Microcode command.

Bit 1 of word 86 shall be set to zero; the CompactFlash Storage Card does not support the Read DMA Queued and Write DMA Queued commands. If bit 2 of word 86 shall be set to one, the CompactFlash Storage Card supports the CFA feature set. If bit 3 of word 86 is set to one, the Advanced Power Management feature set has been enabled via the Set Features command. Bit 4 of word 86 shall be set to zero; the CompactFlash Storage Card does not support the Removable Media Status feature set. Word 88: Ultra DMA Modes Supported and Selected Word 88 identifies the Ultra DMA transfer modes supported by the device and indicates the mode that is currently selected.

Only one DMA mode shall be selected at any given time. If an Ultra DMA mode is selected, then no Multiword DMA mode shall be selected. If a Multiword DMA mode is selected, then no Ultra DMA mode shall be selected. Support of this word is mandatory if Ultra DMA is supported. Bits 15-13: Reserved Bit 12: 1 = Ultra DMA mode 4 is selected 0 = Ultra DMA mode 4 is not selected Bit 11: 1 = Ultra DMA mode 3 is selected 0 = Ultra DMA mode 3 is not selected Bit 10: 1 = Ultra DMA mode 2 is selected 0 = Ultra DMA mode 2 is not selected Bit 9: 1 = Ultra DMA mode 1 is selected 0 = Ultra DMA mode 1 is not selected Bit 8: 1 = Ultra DMA mode 0 is selected 0 = Ultra DMA mode 0 is not selected Bits 7-5: Reserved Bit 4: 1 = Ultra DMA mode 4 and below are supported.



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