10-Bit Multiplying D/A Converter

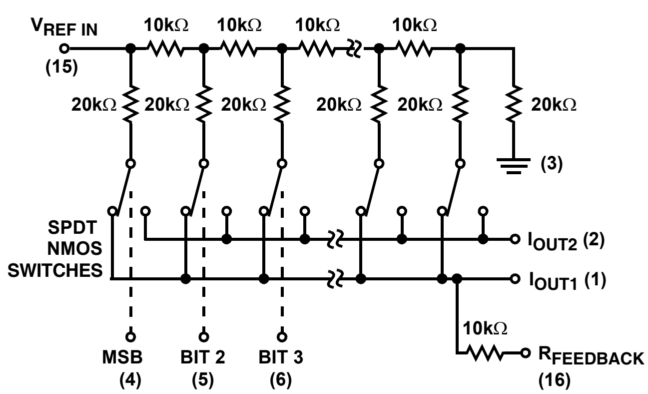
The AD7533 is a monolithic, low cost, high performance, 10-bit accurate, multiplying digital-to-analog converter (DAC), in a 16 pin DIP.

Intersil's thin film resistors on CMOS circuitry provide 10-bit resolution (8-bit accuracy), with TTL/CMOS compatible operation.

The AD7533's accurate four quadrant multiplication, full input protection from damage due to static discharge by clamps to V+ and GND, and very low power dissipation make them very versatile converters.

Low noise audio gain controls, motor speed controls, digitally controlled gain and digital attenuators are a few of the wide range of applications of the AD7533.

Functional Block Diagram



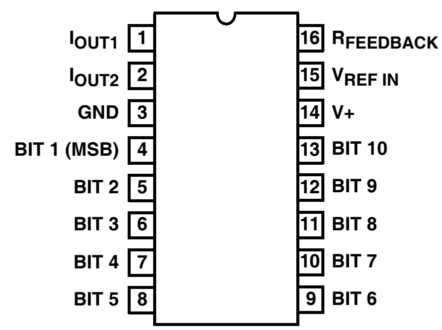
NOTE: Switches shown for digital inputs "High"

Features

- 8-Bit Linearity
- Low Gain and Linearity Temperature Coefficients
- Full Temperature Range Operation
- Static Discharge Input Protection
- TTL/CMOS Compatible
- Supply Range. . . . .+5V to +15V
- Fast Settling Time at 25^{o}C. . . . . 150ns (Max)
- Four Quadrant Multiplication
- AD7533 Direct AD7520 Equivalent

Pinout

AD7533 (PDIP)
TOP VIEW



Ordering Information

PART NUMBER	NUMBER OF BITS	LINEARITY (INL, DNL)	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
AD7533JN	10	0.2% (8-Bit)	0 to 70	16 Ld PDIP	E16.3

Absolute Maximum Ratings

Supply Voltage (V+ to GND) . . . . +17V
V_{REF} . . . . ±25V
Digital Input Voltage Range . . . . V+ to GND
Output Voltage Compliance . . . . -100mV to V+

Operating Conditions

Temperature Range . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
PDIP Package 90
Maximum Junction Temperature (Plastic Package) . . . . 150^oC
Maximum Storage Temperature. . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . 300^oC

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

V+ = +15V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V, Unless Otherwise Specified

PARAMETER		TEST CONDITIONS	T_A 25^oC MIN	T_A 25^oC MAX	T_A MIN-MAX MIN	T_A MIN-MAX MAX	UNITS
SYSTEM PERFORMANCE							
Resolution			10	-	10	-	Bits
Nonlinearity		-10V ≤ V_{REF} ≤ +10V, V_{OUT1} = V_{OUT2} = 0V (Notes 2, 3, 6)	-	±0.2	-	±0.2	% of FSR
Monotonicity			Guaranteed				
Gain Error		All Digital Inputs High (Note 3)	-	±1.4	-	±1.8	% of FSR
Nonlinearity Tempco		-10V ≤ V_{REF} ≤ + 10V (Notes 3, 4)	-	±2	-	±2	ppm of FSR/^oC
Gain Error Tempco			-	±10	-	±10	ppm of FSR/^oC
Output Leakage Current (Either Output)		V_{OUT1} = V_{OUT2} = 0	-	±50	-	±200	nA
DYNAMIC CHARACTERISTICS							
Power Supply Rejection		V+ = 14.0V to 15.0V (Note 3)	-	±0.005	-	±0.008	% of FSR/% of ΔV+
Output Current Settling Time		To 0.2% of FSR, R_L = 100Ω (Note 4)	-	600	-	800	ns
Feedthrough Error		V_{REF} = 20V_{P-P}, 200kHz Sine Wave, All Digital Inputs Low (Note 4)	-	±0.05	-	±0.1	LSB
REFERENCE INPUTS							
Input Resistance (Pin 15)		All Digital Inputs High I_{OUT1} at Ground (Note 4)	5	-	5	-	kΩ
			-	20	-	20	kΩ
Temperature Coefficient			-	-300	-	-300	ppm/^oC
ANALOG OUTPUT							
Output Capacitance	C_{OUT1}	All Digital Inputs High (Note 4)	-	100	-	100	pF
	C_{OUT2}		-	35	-	35	pF
	C_{OUT1}	All Digital Inputs Low (Note 4)	-	35	-	35	pF
	C_{OUT2}		-	100	-	100	pF

Electrical Specifications V+ = +15V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	T_A 25°C		T_A MIN-MAX		UNITS
		MIN	MAX	MIN	MAX	
DIGITAL INPUTS						
Low State Threshold, V_{IL}		-	0.8	-	0.8	V
High State Threshold, V_{IH}		2.4	-	2.4	-	V
Input Current (Low or High), I_{IL}, I_{IH}	V_{IN} = 0V or + 15V	-	±1	-	±1	µA
Input Coding	See Tables 1 through 3	Binary/Offset Binary				
Input Capacitance	(Note 4)	-	4	-	4	pF
POWER SUPPLY CHARACTERISTICS						
Power Supply Voltage Range	(Note 6)	+5 to +16				V
I+	All Digital Inputs High or Low (Excluding Ladder Network)	-	2	-	2.5	mA

NOTES:
2. Full Scale Range (FSR) is 10V for unipolar and ±10V for bipolar modes.
3. Using internal feedback resistor, $R_{FEEDBACK}$.
4. Guaranteed by design or characterization and not production tested.
5. Accuracy not guaranteed unless outputs at ground potential.
6. Accuracy is tested and guaranteed at V+ = +15V, only.

Definition of Terms

Nonlinearity: Error contributed by deviation of the DAC transfer function from a "best straight line" through the actual plot of transfer function. Normally expressed as a percentage of full scale range or in (sub)multiples of 1 LSB.

Resolution: It is addressing the smallest distinct analog output change that a D/A converter can produce. It is commonly expressed as the number of converter bits. A converter with resolution of n bits can resolve output changes of 2^{-N} of the full-scale range, e.g., 2^{-N} V_{REF} for a unipolar conversion. Resolution by no means implies linearity.

Settling Time: Time required for the output of a DAC to settle to within specified error band around its final value (e.g., $^1/_2$ LSB) for a given digital input change, i.e., all digital inputs LOW to HIGH and HIGH to LOW.

Gain Error: The difference between actual and ideal analog output values at full-scale range, i.e., all digital inputs at HIGH state. It is expressed as a percentage of full scale range or in (sub)multiples of 1 LSB.

Feedthrough Error: Error caused by capacitive coupling from V_{REF} to I_{OUT1} with all digital inputs LOW.

Output Capacitance: Capacitance from I_{OUT1}, and I_{OUT2} terminals to ground.

Output Leakage Current: Current which appears on I_{OUT1}, terminal when all digital inputs are LOW or on I_{OUT2} terminal when all digital inputs are HIGH.

For further information on the use of this device, see the following Application Notes:

Application Notes

NOTE #	DESCRIPTION
AN002	"Principles of Data Acquisition and Conversion"
AN018	"Do's and Don'ts of Applying A/D Converters"
AN042	"Interpretation of Data Conversion Accuracy Specifications"

Detailed Description

The AD7533 is a monolithic multiplying D/A converter. A highly stable thin film R-2R resistor ladder network and NMOS SPDT switches form the basis of the converter circuit, CMOS level shifters permit low power TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in the Functional Diagram. The NMOS SPDT switches steer the ladder leg currents between I_{OUT1} and I_{OUT2} buses which must be held at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.

Converter errors are further reduced by using separate metal interconnections between the major bits and the outputs. Use of high threshold switches reduce offset (leakage) errors to a negligible level.

The level shifter circuits are comprised of three inverters with positive feedback from the output of the second to the first, see Figure 1. This configuration results in TTL/CMOS compatible operation over the full military temperature range. With the ladder SPDT switches driven by the level shifter, each switch is binarily weighted for an ON resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors and high accurate leg currents.

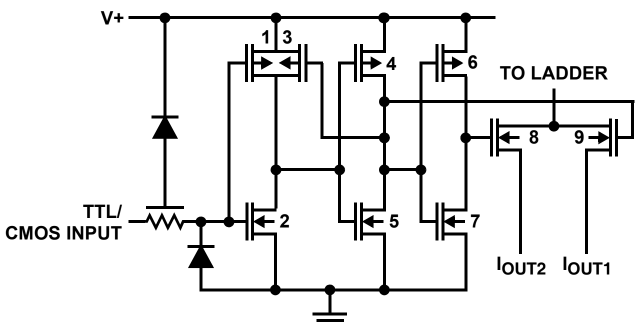
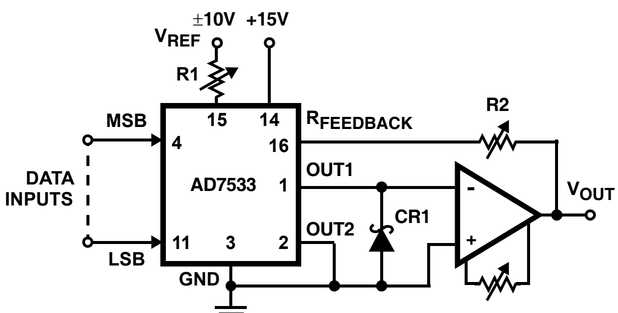


FIGURE 1. CMOS SWITCH

Typical Applications



NOTES:

7. R1 and R2 used only if gain adjustment is required.
8. CR1 protects AD7533 against negative transients.

FIGURE 2. UNIPOLAR BINARY OPERATION

Unipolar Binary Operation - (10-Bit DAC)

The circuit configuration for operating the AD7533 in unipolar mode is shown in Figure 2. With positive and negative V_{REF} values the circuit is capable of 2-Quadrant multiplication. The “Digital Input Code/Analog Output Value” table for unipolar mode is given in Table 1.

TABLE 1. UNIPOLAR BINARY CODE - AD7533

DIGITAL INPUT MSB LSB	(NOTE 9) NOMINAL ANALOG OUTPUT
1111111111	$-V_{REF}\left(\frac{1023}{1024}\right)$
1000000001	$-V_{REF}\left(\frac{513}{1024}\right)$
1000000000	$-V_{REF}\left(\frac{512}{1024}\right) = -\frac{V_{REF}}{2}$
0111111111	$-V_{REF}\left(\frac{511}{1024}\right)$
0000000001	$-V_{REF}\left(\frac{1}{1024}\right)$
0000000000	$-V_{REF}\left(\frac{0}{1024}\right) = 0$

TABLE 1. UNIPOLAR BINARY CODE - AD7533

NOTES:

9. V_{OUT} as shown in Figure 2.
10. Nominal Full Scale for the circuit of Figure 2 is given by:

$$FS = -V_{REF}\left(\frac{1023}{1024}\right).$$

11. Nominal LSB magnitude for the circuit of Figure 2 is given by:

$$LSB = V_{REF}\left(\frac{1}{1024}\right).$$

Zero Offset Adjustment

1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V ±1mV (Max) at V_{OUT}.

Gain Adjustment

1. Connect all digital inputs to V+.
2. Monitor V_{OUT} for a $-V_{REF}$ $(1 - 1/2^{10})$ reading.
3. To increase V_{OUT}, connect a series resistor, R2, (0Ω to 250Ω) in the I_{OUT1} amplifier feedback loop.
4. To decrease V_{OUT}, connect a series resistor, R1, (0Ω to 250Ω) between the reference voltage and the V_{REF} terminal.

Bipolar (Offset Binary) Operation

The circuit configuration for operating the AD7533 in the bipolar mode is given in Figure 3. Using offset binary digital input codes and positive and negative reference voltage values, 4-Quadrant multiplication can be realized. The “Digital Input Code/Analog Output Value” table for bipolar mode is given in Table 2.

A “Logic 1” input at any digital input forces the corresponding ladder switch to steer the bit current to I_{OUT1} bus. A “Logic 0” input forces the bit current to I_{OUT2} bus. For any code the I_{OUT1} and I_{OUT2} bus currents are complements of one another. The current amplifier at I_{OUT2} changes the polarity of I_{OUT2} current and the transconductance amplifier at I_{OUT1} output sums the two currents. This configuration doubles the output range. The difference current resulting at zero offset binary code, (MSB = “Logic 1”, all other bits = “Logic 0”), is corrected by using an external resistor, (10MΩ), from V_{REF} to I_{OUT2}.

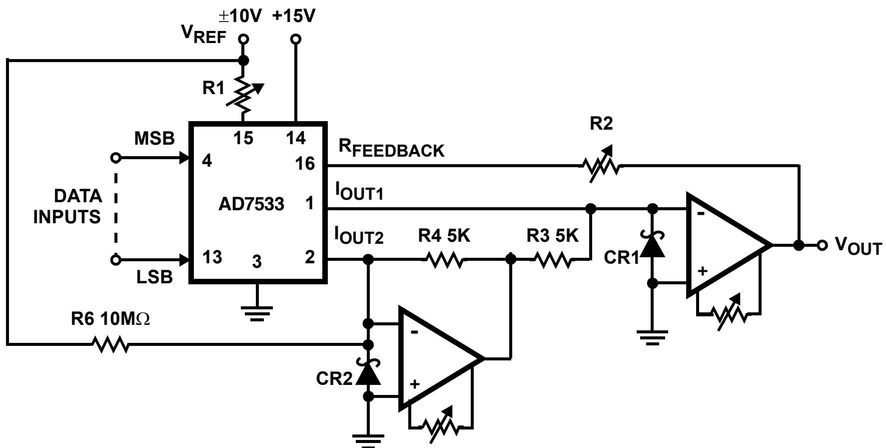


FIGURE 3. BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

TABLE 2. UNIPOLAR BINARY CODE - AD7533

DIGITAL INPUT MSB LSB	(NOTE 2) NOMINAL ANALOG OUTPUT
1111111111	$-V_{REF}\left(\frac{511}{512}\right)$
1000000001	$-V_{REF}\left(\frac{1}{512}\right)$
1000000000	0
0111111111	$+V_{REF}\left(\frac{1}{512}\right)$
0000000001	$+V_{REF}\left(\frac{511}{512}\right)$
0000000000	$+V_{REF}\left(\frac{512}{512}\right)$

NOTES:

12. V_{OUT} as shown in Figure 3.
13. Nominal Full Scale for the circuit of Figure 3 is given by:

$$FSR = V_{REF}\left(\frac{1023}{512}\right).$$

14. Nominal LSB magnitude for the circuit of Figure 3 is given by:

$$LSB = V_{REF}\left(\frac{1}{512}\right).$$

Offset Adjustment

5. Adjust V_{REF} to approximately +10V.
6. Connect all digital inputs to “Logic 1”.
7. Adjust I_{OUT2} amplifier offset adjust trimpot for 0V ±1mV at I_{OUT2} amplifier output.
8. Connect MSB (Bit 1) to “Logic 1” and all other bits to “Logic 0”.
9. Adjust I_{OUT1} amplifier offset adjust trimpot for 0V ±1mV at V_{OUT}.

Gain Adjustment

1. Connect all digital inputs to V+.
2. Monitor V_{OUT} for a $-V_{REF}$ $(1 - 2^{-9})$ volts reading.
3. To increase V_{OUT}, connect a series resistor (R2) of up to 250Ω between V_{OUT} and $R_{FEEDBACK}$.
4. To decrease V_{OUT}, connect a series resistor (R1) of up to 250Ω between the reference voltage and the V_{REF} terminal.

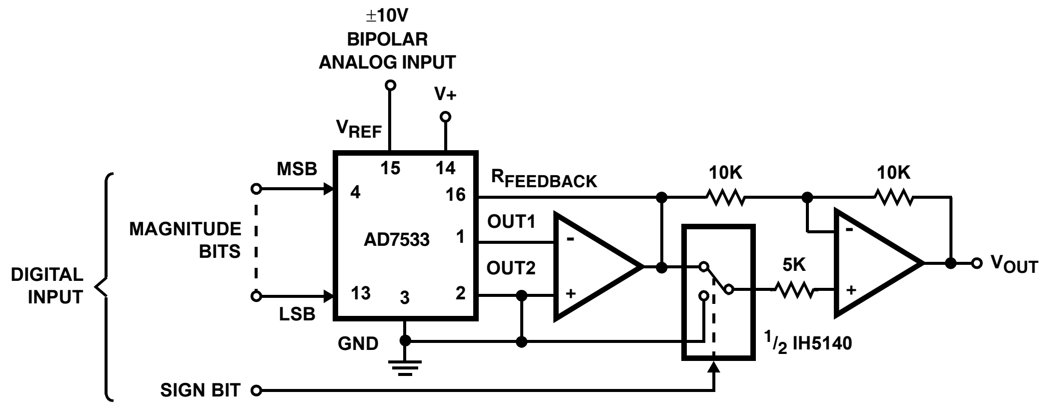


FIGURE 4. 10-BIT AND SIGN MULTIPLYING DAC

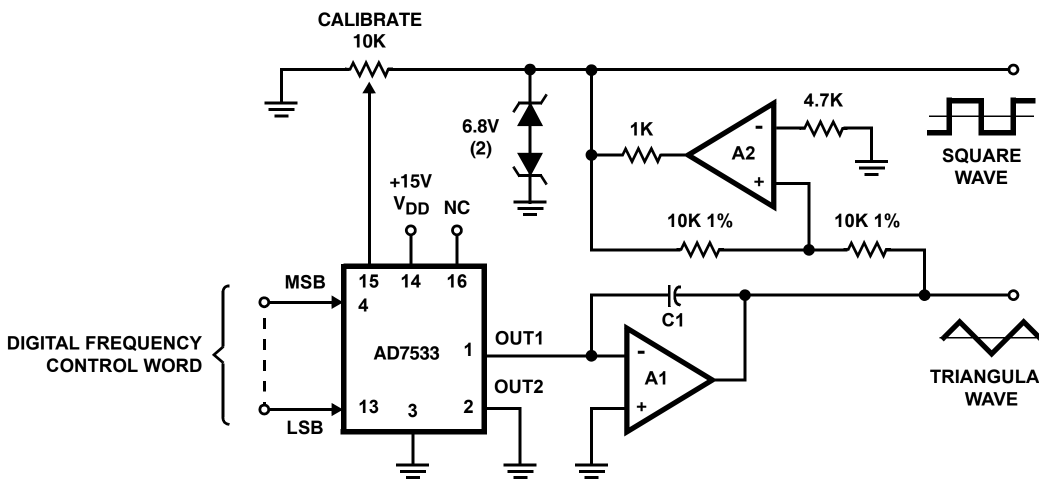
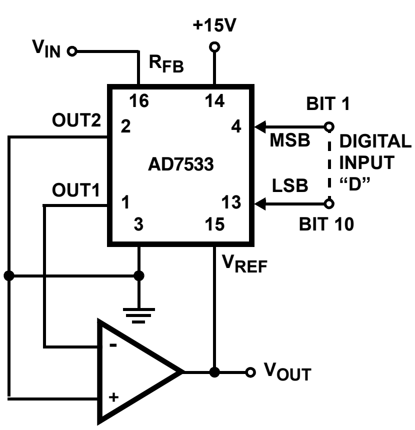


FIGURE 5. PROGRAMMABLE FUNCTION GENERATOR



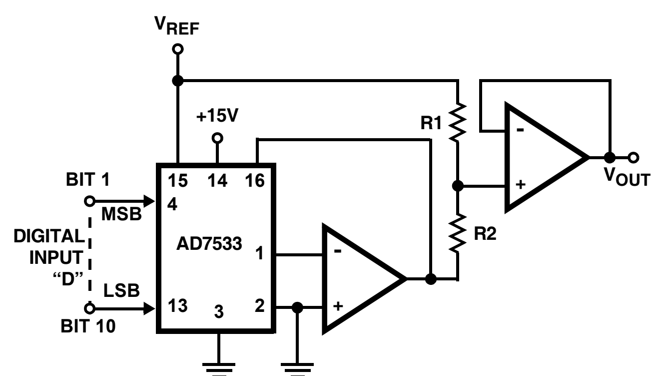
$V_{OUT} = -V_{IN/D}$

Where:

$$D = \frac{\text{Bit 1}}{2^1} + \frac{\text{Bit 2}}{2^2} + \ldots \frac{\text{Bit 8}}{2^2}$$

$$\left(0 \le D \le \frac{255}{256}\right)$$

FIGURE 6. DIVIDER (DIGITALLY CONTROLLED GAIN)



$$V_{OUT} = V_{REF}\left[\left(\frac{R_2}{R_1 + R_2}\right) - \left(\frac{R_1 D}{R_1 + R_2}\right)\right]$$

$$\text{Where } D = \frac{\text{Bit 1}}{2^1} + \frac{\text{Bit 2}}{2^2} + \ldots \frac{\text{Bit 8}}{2^8}$$

$$\left(0 \le D \le \frac{255}{256}\right)$$

FIGURE 7. MODIFIED SCALE FACTOR AND OFFSET

Die Characteristics

DIE DIMENSIONS

101 mils x 103 mils (2565μm x 2616μm)

METALLIZATION

Type: Pure Aluminum
Thickness: 10 ±1kÅ

PASSIVATION

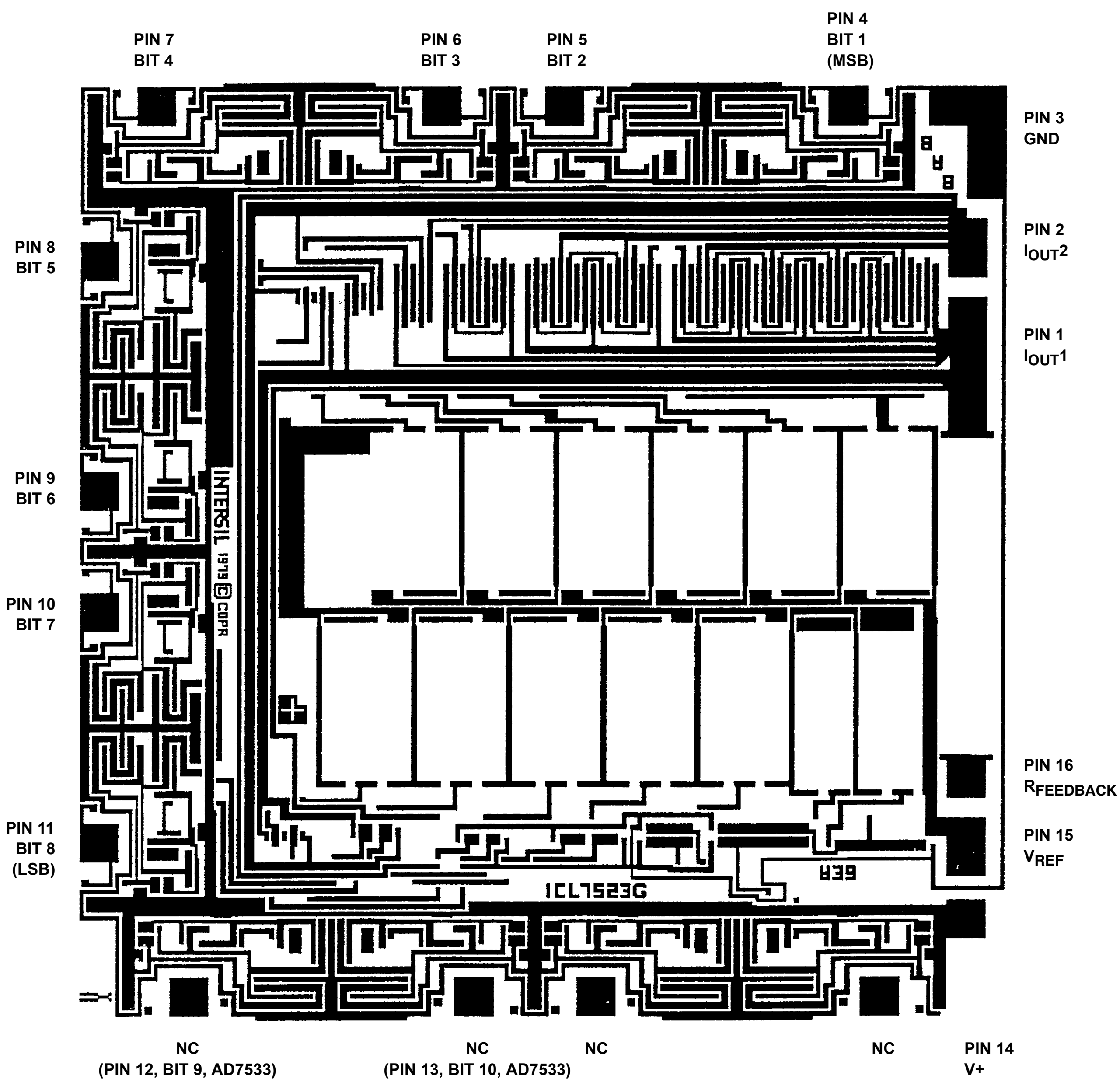
Type: PSG/Nitride
PSG: 7 ±1.4kÅ
Nitride: 8 ±1.2kÅ

PROCESS

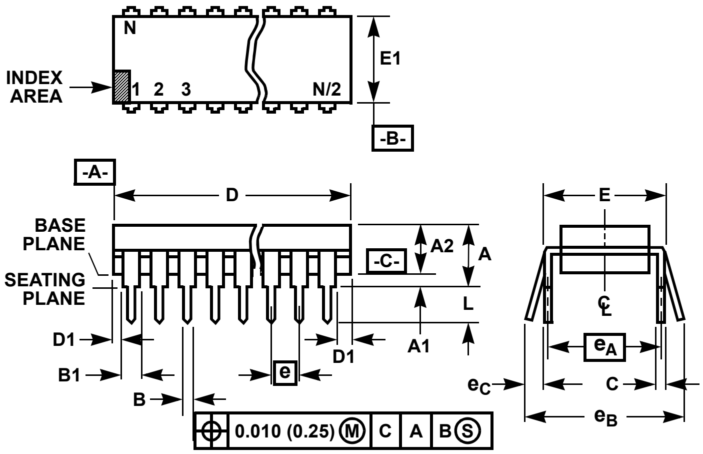
CMOS Metal Gate

Metallization Mask Layout

AD7533



Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and $\boxed{e_A}$ are measured with the leads constrained to be perpendicular to datum $\boxed{\text{-C-}}$.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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